

DESCRIPTION

REPRODUCING APPARATUS AND METHOD, RECORDING MEDIUM, AND
PROGRAM

5

TECHNICAL FIELD

[0001]

The present invention relates to a reproducing
apparatus and method, a recording medium, and a program,
10 and more particularly to a reproducing apparatus and
method, a recording medium, and a program, all capable of
reducing more errors caused by so-called bit slips.

BACKGROUND ART

15 [0002]

A reproducing apparatus, such as an optical disc
apparatus, a HDD (Hard Disk Drive), a digital video
cassette or a data streamer, generates a clock from a
reproduced signal acquired by reading a recording medium,
20 and processes the reproduced signal using the generated
clock, to reproduce data recorded on the recording medium.

[0003]

Fig. 1 is a diagram showing a conventional
configuration of a reproducing apparatus for recording
25 media.

[0004]

An equalizer 11 shapes a reproduced signal from a
recording medium, and the reproduced signal is supplied
to an A/D converter (Analog/Digital converter) 12.

30 [0005]

The A/D converter 12 converts the reproduced signal,

which is an analog signal supplied from the equalizer 11 into digital signals on the basis of reproduced clocks to be supplied from a clock generation section 13, and supplies the digital signals generated after the
5 conversion, to the clock generation section 13 and an equalizer 14.

[0006]

The clock generation section 13 includes a phase error detecting section 21 and a VCO (Voltage Controlled
10 Oscillator) 22, and generates reproduced clocks using a PLL (Phase Locked Loop) system. The reproduced clocks are supplied to the A/D converter 12, the clock generation section 13, the equalizer 14 and a data detecting section 15.

15 [0007]

A phase error integrating section 21 detects a phase error between a reproduced clock and the corresponding digital signal outputted from the A/D converter 12, and supplies a signal corresponding to the
20 phase error, to the VCO 22.

[0008]

The VCO 22 outputs a reproduced clock having such a frequency as to reduce the phase error, on the basis of the signal from the phase error detecting section 21.
25 The reproduced clock is supplied further to the phase error detecting section 21.

[0009]

The equalizer 14 shapes the digital signal on the basis of the reproduced clock, and supplies the shaped
30 digital signal to the data detecting section 15.

[0010]

The data detecting section 15 corrects the digital signal error by Viterbi decoding, and outputs the error-corrected digital signal as detected data.

[0011]

5 When the recording medium has a defect, there occurs a deviation, i.e., a so-called bit slip, between a clock generated and data reproduced, from an input signal. When the bit slip has occurred, the error propagates to the subsequent data, leaving the error uncorrectable.

10 [0012]

In order to avoid such a situation, specific patterns called synchronization patterns are arranged at predetermined intervals in the recording medium, whereby to prevent propagation of the error caused by the bit
15 slip using the synchronization patterns.

[0013]

There has been proposed a synchronization circuit (e.g., see Patent Document 1), in which: a synchronization pattern is detected from a digital
20 signal; clock pulses are counted; a predicted synchronization pattern position is set on the basis of a count value; a predicted synchronization pattern range is set on the basis of the count value; a count value is held; a sync signal is outputted by referring to the
25 detected synchronization pattern, the count value, the predicted synchronization pattern position, the set synchronization pattern range and the count value held, and the counter is reset by this sync signal. In this synchronization circuit, in a case where a
30 synchronization pattern has been detected within the set predicted range, a sync signal is outputted at a timing

at which the synchronization pattern has been detected,
whereas in a case where no synchronization pattern has
been detected within the set predicted range, a sync
signal is outputted at the set timing. Moreover, in a
5 case where a synchronization pattern has been detected
beyond the set predicted range, a count value in the
counter is compared with a count value held, and if both
counts coincide, a sync signal is outputted at that
timing, whereas if both count values do not coincide, the
10 count in the counter is held.

[0014]

Furthermore, there has been a synchronization
circuit in which a phase deviation in a reproduced clock
generated from a reproduced signal is detected, and any
15 loss or gain in the reproduced signal is outputted as a
bit slip detection signal, on the basis of this phase
deviation, whereby to prevent propagation of an error
caused by a bit slip (see Patent Document 2).

[0015]

20 [Patent Document 1]

Japanese Patent Application Publication No. 8-
212705

[0016]

[Patent Document 2]

25 Japanese Patent Application Publication No. 10-
255409

[0017]

However, amidst growing incidences of signal
defects due to dust and blemishes as the recording
30 densities in recording media increase, prevention of
propagation of burst errors merely with synchronization

patterns is not enough to guarantee stable reading of data recorded on recording media.

[0018]

Moreover, there may actually be cases where no
5 synchronization pattern is detected throughout phase locking in the PLL after a bit slip has occurred due to a signal defect, and thus, despite the fact that the reproduced signal itself has recovered, the burst error propagates further to a next synchronization pattern,
10 thus elevating the error rate.

[Means for Solving the Problems]

[0019]

A reproducing apparatus of the present invention is characterized by including: synchronization pattern
15 detecting means for detecting a synchronization pattern which is detected from a reproduced signal from a data storage medium and which is contained in data; error detecting means for detecting an error between the reproduced signal and a reference point specified by a
20 time at which a half cycle has elapsed from a start time of one cycle of a clock signal reproduced from the reproduced signal, and by an amplitude of the reproduced signal; and correcting means for correcting a deviation of the data from the clock signal, on the basis of a
25 difference between an interval of the synchronization pattern detected and a predetermined period, and of a time for a segment in which it is assumed, from the error detected, that the deviation of the data from the clock signal has occurred, out of segments into which the
30 interval of the synchronization pattern is divided.

[0020]

The synchronization pattern detecting means may include: detection range setting means for setting a detection range from which the synchronization pattern is detected, on the basis of a count value of the clock signal; and synchronization pattern detection signal inserting means for inserting a signal representing detection of the synchronization pattern, at a time specified by the predetermined period, where the synchronization pattern has not been detected within the detection range.

[0021]

The error detecting means may detect a phase error, which is an error in a time direction between the reference point and the reproduced signal, and the correcting means may correct the deviation of the data from the clock signal, on the basis of the difference between the interval of the synchronization pattern detected and the predetermined period, and of the time for the segment in which it is assumed, from the phase error detected, that the deviation of the data from the clock signal has occurred, out of the segments into which the interval of the synchronization pattern is divided.

[0022]

The error detecting means may detect a zero-crossing offset, which is an error in an amplitude direction between the reference point and the reproduced signal, and the correcting means may correct the deviation of the data from the clock signal, on the basis of the difference between the interval of the synchronization pattern detected and the predetermined period, and of the time for the segment in which it is

assumed, from the zero-crossing offset detected, that the deviation of the data from the clock signal has occurred, out of the segments into which the interval of the synchronization pattern is divided.

5 [0023]

The correcting means may include: deviation amount detecting means for detecting the difference between the interval of the synchronization pattern and the predetermined period, on the basis of the clock signal, as a deviation amount; error integrating means for integrating the error for each of the segments; deviation occurrence time detecting means for detecting a deviation occurrence time, which is a time for the segment in which an absolute value of the integrated value integrated becomes maximum between two successive ones of the synchronization patterns; a FIFO (First In First Out) buffer for storing the data equivalent to a period longer than the predetermined period; and control means for controlling the FIFO buffer such that the data equivalent to a period from the deviation occurrence time to detection of the synchronization pattern is moved in a time direction so as to correspond to the deviation amount, on the basis of the deviation amount and the deviation occurrence time, in a case where the deviation amount other than 0 has been detected.

25 [0024]

A reproducing method of the present invention is characterized by including: a synchronization pattern detecting step of detecting a synchronization pattern which is detected from a reproduced signal from a data storage medium and which is contained in data; an error

detecting step of detecting an error between the reproduced signal and a reference point specified by a time at which a half cycle has elapsed from a start time of one cycle of a clock signal reproduced from the reproduced signal, and by an amplitude of the reproduced signal; and a correcting step of correcting a deviation of the data from the clock signal, on the basis of a difference between an interval of the synchronization pattern detected and a predetermined period, and of a time for a segment in which it is assumed, from the error detected, that the deviation of the data from the clock signal has occurred, out of segments into which the interval of the synchronization pattern is divided.

[0025]

15 A program for a recording medium of the present invention is characterized by including: a synchronization pattern detecting step of detecting a synchronization pattern which is detected from a reproduced signal from a data storage medium and which is contained in data; an error detecting step of detecting an error between the reproduced signal and a reference point specified by a time at which a half cycle has elapsed from a start time of one cycle of a clock signal reproduced from the reproduced signal, and by an amplitude of the reproduced signal; and a correcting step of correcting a deviation of the data from the clock signal, on the basis of a difference between an interval of the synchronization pattern detected and a predetermined period, and of a time for a segment in which it is assumed, from the error detected, that the deviation of the data from the clock signal has occurred,

out of segments into which the interval of the
synchronization pattern is divided.

[0026]

A program of the present invention is characterized
5 by including: a synchronization pattern detecting step of
detecting a synchronization pattern which is detected
from a reproduced signal from a data storage medium and
which is contained in data; an error detecting step of
detecting an error between the reproduced signal and a
10 reference point specified by a time at which a half cycle
has elapsed from a start time of one cycle of a clock
signal reproduced from the reproduced signal, and by an
amplitude of the reproduced signal; and a correcting step
of correcting a deviation of the data from the clock
15 signal, on the basis of a difference between an interval
of the synchronization pattern detected and a
predetermined period, and of a time for a segment in
which it is assumed, from the error detected, that the
deviation of the data from the clock signal has occurred,
20 out of segments into which the interval of the
synchronization pattern is divided.

[0027]

In the reproducing apparatus and method, the
recording medium and the program of the present invention,
25 a synchronization pattern which is detected from a
reproduced signal from a data storage medium and which is
contained in data is detected, and an error between the
reproduced signal and a reference point specified by a
time at which a half cycle has elapsed from a start time
30 of one cycle of a clock signal reproduced from the
reproduced signal, and by an amplitude of the reproduced

signal is detected. And a deviation of the data from the clock signal is corrected on the basis of a difference between an interval of the synchronization pattern detected and a predetermined period, and of a time for a segment in which it is assumed, from the error detected, that the deviation of the data from the clock signal has occurred, out of segments into which the interval of the synchronization pattern is divided.

10 BRIEF DESCRIPTION OF THE DRAWINGS

[0028]

[Fig. 1] It is a block diagram showing a conventional reproducing apparatus.

[Fig. 2] It is a block diagram showing a configuration of an embodiment of a reproducing apparatus of the present invention.

[Fig. 3] It is a block diagram showing details of a synchronization detecting section and a bit slip correcting section.

[Fig. 4] It is a diagram for explaining phase error detection.

[Fig. 5] It is a timing chart showing detection of a deviation amount and a time at which the deviation is predicted to have occurred, with respect to successive synchronization patterns, in a case where a bit slip has occurred.

[Fig. 6] It is a diagram showing a method of calculating a bit slip occurrence position, in the case where a bit slip has occurred.

[Fig. 7] It is a timing chart for explaining insertion of a synchronization pattern detection signal,

in a case where no synchronization pattern has been detected in a synchronization pattern interpolation mode.

[Fig. 8] It is a diagram showing a method of calculating a bit slip occurrence position, in a case
5 where the synchronization pattern has been interpolated.

[Fig. 9] It is a flowchart for explaining a reproduction process.

[Fig. 10] It is a flowchart for explaining bit slip correction.

10 [Fig. 11] It is a flowchart for explaining details of synchronization pattern detection.

[Fig. 12] It is a flowchart for explaining details of a correction information calculating process.

[Fig. 13] It is a flowchart for explaining
15 details of a FIFO control process.

[Fig. 14] It is a diagram for explaining detected data correction.

[Fig. 15] It is a diagram for explaining detected data correction.

20 [Fig. 16] It is a diagram for explaining detected data correction.

[Fig. 17] It is a diagram for explaining detected data correction.

[Fig. 18] It is a block diagram showing another
25 configuration of an embodiment of the reproducing apparatus of the present invention.

[Fig. 19] It is a block diagram showing details of a synchronization detecting section and a bit slip correcting section.

30 [Fig. 20] It is a diagram for explaining zero-crossing offset detection.

[Fig. 21] It is a timing chart showing detection of a deviation amount and a time at which the deviation is predicted to have occurred, with respect to successive synchronization patterns, in a case where a bit slip has occurred.

[Fig. 22] It is a diagram showing a method of calculating a bit slip occurrence position, in the case where a bit slip has occurred.

[Fig. 23] It is a timing chart for explaining insertion of a synchronization pattern detection signal, in a case where no synchronization pattern has been detected in a synchronization pattern interpolation mode.

[Fig. 24] It is a diagram showing a method of calculating a bit slip occurrence position, in a case where the synchronization pattern has been interpolated.

[Fig. 25] It is a flowchart for explaining a reproduction process.

[Fig. 26] It is a flowchart for explaining bit slip correction.

[Fig. 27] It is a flowchart for explaining details of a correction information calculating process.

[Description of Reference Numerals]

[0029]

31: equalizer, 32: A/D converting section, 33: clock generating section, 34: equalizer, 35: data detecting section, 36: error correcting section, 41: phase error detecting section, 42: VCO, 51: phase error detecting section, 52: synchronization detecting section, 53: bit slip correcting section, 61: drive, 71: magnetic disk, 72: optical disc, 73: magneto-optical disc, 74: semiconductor memory, 81: bit slip judging section, 82:

FIFO control section, 83: FIFO, 84: detection range
setting section, 85: synchronization pattern detection
signal inserting section, 91: synchronization pattern
interval counter, 92: phase error integrating section,
5 93: maximum phase error time storing section, 301: zero-
crossing offset detecting section, 302: bit slip
correcting section, 311: bit slip judging section, 321:
zero-crossing offset integrating section, 322: maximum
zero-crossing offset time storing section

10

BEST MODES FOR CARRYING OUT THE INVENTION

[0030]

In the following description of the best modes of
the present invention, inventions to be disclosed
15 correspond to embodiments as follows, by way of example.
The presence of an embodiment described in the present
Specification but not described herein as corresponding
to an invention should not mean that the embodiment does
not correspond to the invention. Conversely, a
20 description of an embodiment herein as corresponding to
an invention should not mean that the embodiment does not
correspond to an invention or inventions other than that
invention.

[0031]

25 Furthermore, this description does not comprehend
all the inventions described in the Specification. In
other words, this description does not deny the presence
of an invention or inventions described in the
Specification but not claimed in the present application,
30 i.e., the presence of an invention or inventions to be
appearing or added due to divisional application(s) or

correction(s).

[0032]

Embodiments of the present invention will be described below with reference to the drawings.

5 [0033]

Fig. 2 is a block diagram showing a configuration of an embodiment of a reproducing apparatus of the present invention.

[0034]

10 An equalizer 31 shapes a reproduced signal which a pickup, not shown, has reproduced from a recording medium such as an optical disc, a hard disk or a digital video cassette, and supplies the reproduced signal thus reproduced to an A/D converting section 32. This
15 recording medium is an example of a data storage medium, and may thus include any medium that records data by chemical or physical change and is mechanically driven for reproduction.

[0035]

20 The A/D converting section 32 converts the reproduced signal, which is an analog signal supplied from the equalizer 31, into digital signals on the basis of reproduced clocks to be supplied from a clock generating section 33. The A/D converting section 32
25 supplies the digital signals generated through the conversion, to the clock generating section 33 and an equalizer 34.

[0036]

The clock generating section 33 includes a phase
30 error detecting section 41 and a VCO 42, and generates the reproduced clocks from the digital signals using the

PLL system.

[0037]

The phase error detecting section 41 detects a phase error between a reproduced clock and the
5 corresponding digital signal outputted from the A/D converting section 32, and supplies a signal representing the magnitude of the phase error, to the VCO 42.

[0038]

The VCO 42 changes an oscillating frequency so as
10 to correspond to the magnitude of the phase error on the basis of the corresponding signal from the phase error detecting section 41, to output a reproduced clock of such a frequency reducing the phase error more. The reproduced clock is supplied to the A/D converting
15 section 32, the phase error detecting section 41, a phase error detecting section 51, a synchronization detecting section 52 and a bit slip correcting section 53.

[0039]

The equalizer 34 adjusts the edge position of the
20 digital signal in the time direction on the basis of the corresponding reproduced clock, to shape the digital signal, and supplies the shaped digital signal to a data detecting section 35 and an error correcting section 36.

[0040]

25 The shaped digital signal will hereinafter be referred to also as "equalized amplitude information".

[0041]

The data detecting section 35 corrects the digital signal error by means of Viterbi decoding, and outputs
30 the error-corrected digital signal as detected data.
Note that the data detecting section 35 may alternatively

utilize a maximum-likelihood decoding system other than Viterbi decoding.

[0042]

5 The error correcting section 36 includes the phase error detecting section 51, the synchronization detecting section 52 and the bit slip correcting section 53.

[0043]

10 The phase error detecting section 51 detects a phase error between equalized amplitude information supplied from the equalizer 34 and the corresponding reproduced clock, and supplies a phase error signal representing the phase error, to the bit slip correcting section 53.

[0044]

15 The synchronization detecting section 52 detects a synchronization pattern composed of a predetermined bit pattern on the basis of detected data and the corresponding reproduced clocks, and supplies a synchronization pattern detection signal indicating that a synchronization pattern has been detected, to the bit slip correcting section 53.

[0045]

25 The bit slip correcting section 53 corrects an error caused by a bit slip, on the basis of the detected data, the phase error signal, the synchronization pattern detection signal, and the reproduced clock, and outputs the corrected detected data.

[0046]

30 A drive 61 is connected to the reproducing apparatus, as necessary. A magnetic disk 71, an optical disc 72, a magneto-optical disc 73 or a semiconductor

memory 74 attached is attached to the drive 61, whenever appropriate. The drive 61 reads a program stored in the magnetic disk 71, optical disc 72, magneto-optical disc 73 or semiconductor memory 74 attached, and supplies the
5 read program to the error correcting section 36.

[0047]

Thus, the error correcting section 36 can execute the program read from the magnetic disk 71, optical disc 72, magneto-optical disc 73 or semiconductor memory 74,
10 which is an example of the recording medium.

[0048]

Note that the detected data outputted from the bit slip correcting section 53 is decoded by a predetermined system such as EFM (Eight to Fourteen Modulation), and
15 error-corrected by, e.g., ECC (Error Correction Coding).

[0049]

Fig. 3 is a block diagram showing configurational details of the synchronization detecting section 52 and the bit slip correcting section 53.

20 [0050]

The bit slip correcting section 53 includes a bit slip judging section 81, a FIFO control section 82 and a FIFO buffer 83. Moreover, the synchronization detecting section 52 includes a detection range setting section 84
25 and a synchronization pattern detection signal inserting section 85.

[0051]

Furthermore, the bit slip judging section 81 includes a synchronization pattern interval counter 91, a
30 phase error integrating section 92 and a maximum phase error time storing section 93.

[0052]

The detection range setting section 84 sets a detection range from which a synchronization pattern is to be detected, on the basis of a reproduced clock signal count value.

[0053]

The synchronization pattern detection signal inserting section 85 inserts a synchronization pattern detection signal at a predetermined period, in a case where no synchronization pattern is detected within the detection range. Here, "the predetermined period" means each of equal intervals at which specific patterns as synchronization patterns, which are different from recorded data, are usually embedded in a recorded signal, generally in a recording medium (data storage medium) such as an optical disc. Therefore, the period at which the synchronization pattern detection signal is inserted is determined by the format of a recording medium.

[0054]

The bit slip judging section 81 detects a deviation amount between a reproduced clock and the corresponding detected data on the basis of a synchronization pattern detection signal supplied from the synchronization detecting section 52 and the phase error signal supplied from the phase error detecting section 51, and also specifies a time at which the deviation between the reproduced clock and the detected data is predicted to have occurred. The bit slip judging section 81 supplies a signal representing the deviation amount between the reproduced clock and the detected data and a signal representing the time at which the deviation is predicted

to have occurred, to the FIFO control section 82.

[0055]

The signal representing the deviation amount between the reproduced clock and the detected data and the signal representing the time at which the deviation is predicted to have occurred will hereinafter be referred to also as "bit slip correction information".

[0056]

The synchronization pattern interval counter 91 detects a difference between the predetermined period and the sync signal detected by the synchronization detecting section 51 on the basis of the reproduced clock, as the deviation amount.

[0057]

The phase error integrating section 92 integrates phase errors detected within each of segments into which an interval between two successive synchronization patterns is divided, whereby to calculate a phase error segment integrated value. Here, a segment into which the interval is divided is determined by any of the predetermined number of phase errors, a predetermined period and predetermined channel bits.

[0058]

The maximum phase error time storing section 93 detects a time at which a deviation between a reproduced clock and equalized amplitude information is predicted to have occurred, which is a time defining a segment in which the absolute value of an integrated value obtained by integration becomes maximum between two successive synchronization patterns, and stores that time.

[0059]

The FIFO control section 82 controls the FIFO buffer 83 on the basis of the signal representing the deviation amount between the reproduced clock and the detected data supplied from the bit slip judging section 81, and the signal representing the time at which the deviation is predicted to have occurred, whereby to cause the FIFO buffer 83 to correct the deviation of the stored detected data from the corresponding reproduced clock.

[0060]

10 The FIFO buffer 83 is a First-In First-Out buffer for storing an amount of detected data larger than the number of detected data bits arranged between two synchronization patterns. The FIFO buffer 83 moves the detected data in the time direction so as to correspond to the deviation amount on the basis of control information supplied from the FIFO control section 82, whereby to perform bit slip correction to output the corrected data as detected data.

[0061]

20 Note that the phase error integrating section 92 may alternatively average phase errors detected in each of the segments into which the interval between two successive synchronization patterns is divided, whereby to calculate a phase error segment average.

25 [0062]

Referring next to Fig. 4, an example of phase error detection in the phase error detecting section 51 will be described.

[0063]

30 Fig. 4 is a diagram showing a signal waveform of reproduced clocks, detected data which can take either

"1" or "0", and values of equalized amplitude information, with a time axis t extending in the horizontal direction. In Fig. 4, $\text{data}(n-1)$ and $\text{data}(n)$ are amplitude values of the equalized amplitude information at the rises of the reproduced clocks, respectively. The " $\text{data}(n)$ " is the amplitude value of the equalized amplitude information next to the " $\text{data}(n-1)$ ".

[0064]

A phase error is calculated by, e.g., the following equation (1).

[0065]

$$\text{Phase error} = [\text{data}(n) + \text{data}(n-1)] / [\text{data}(n) - \text{data}(n-1)] \cdots (1)$$

[0066]

From the equation (1), a deviation amount in terms of time of the equalized amplitude information from each corresponding reproduced clock can be calculated.

[0067]

In a case where there is no phase error, a time when signs of equalized amplitude information switch coincides with a time t_0 at which "1" switches to "0" in the corresponding reproduced clock. A difference (error) between the time t_0 at which "1" switches to "0" in the reproduced clock and the time at which the polarities (signs) of the equalized amplitude information switch is a phase error. The arrow in Fig. 4 represents a phase error.

[0068]

That is, as shown in Fig. 4, in one cycle of the reproduced clock, detected data takes either one of the values "1" and "0". For example, one cycle of the

reproduced clock is defined to extend from a rise of a reproduced clock to the next rise of the reproduced clock. It can be said that the rises of reproduced clocks represent the start time and the end time of one cycle of the reproduced clock. In this case, a reproduced clock falls at the time t_0 at which a $1/2$ cycle of the reproduced clock (half cycle) has elapsed from the start time of one cycle of the reproduced clock. The time t_0 at which a $1/2$ cycle of the reproduced clock has elapsed from the start time of one cycle of the reproduced clock will hereinafter be referred to as "half cycle point".

[0069]

Here, a relationship between time and amplitude value of equalized amplitude information will be considered. In the lower side of Fig. 4, the horizontal direction represents time, and the vertical direction represents amplitude value of equalized amplitude information.

[0070]

In a case where no error is contained in equalized amplitude information, i.e., where equalized amplitude information is ideal, in a coordinate space having time and amplitude value of equalized amplitude information as its coordinate axes, respectively, a straight line connecting a point specified by the start time of a certain cycle of the reproduced clock and the amplitude value $\text{data}(n-1)$ of the equalized amplitude information at that start time, with a point specified by the start time of a next cycle of the reproduced clock and the amplitude value $\text{data}(n)$ of the equalized amplitude information at the start time of the next cycle passes through a point

specified by the half cycle point and an amplitude value which is 0.

[0071]

That is, in a case where no error is contained in
5 the equalized amplitude information, this straight line
and a straight line representing the amplitude value
which is 0 cross at the half cycle point (time t_0).

[0072]

In a case where an error is contained in equalized
10 amplitude information, in a coordinate space having time
and amplitude value of equalized amplitude information as
its coordinate axes, respectively, a straight line
connecting a point specified by the start time of a
certain cycle of the reproduced clock and the amplitude
15 value data(n-1) of the equalized amplitude information at
that start time, with a point specified by the start time
of a next cycle of the reproduced clock and the amplitude
value data(n) of the equalized amplitude information at
the start time of the next cycle does not pass through a
20 point specified by the half cycle point and an amplitude
value which is 0. In a case where an error is contained
in the equalized amplitude information, the point at
which this straight line crosses the straight line
representing the amplitude value which is 0 deviates from
25 the half cycle point (time t_0) in the time direction.

[0073]

The point at which this straight line crosses the
straight line representing the amplitude value which is 0
in the coordinate space having time and amplitude value
30 of equalized amplitude information as its coordinate axes,
respectively, will hereinafter be referred to as "phase

error point".

[0074]

That is, the phase error detecting section 51 detects an error (e.g., the arrow in Fig. 4) between the error reference point and the phase error point as a phase error.

[0075]

Here, it is necessary that the polarity of the amplitude value data(n-1) of the equalized amplitude information and the polarity of the amplitude value data(n) of the equalized amplitude information, in a case where a phase error has been detected, are different.

[0076]

Note that in the equation (1), the time axis direction may be arbitrarily selectable. In this case, data(n) and data(n-1) in the denominator of the equation (1) may be switched in sequence.

[0077]

Moreover, the denominator of the equation (1) may take a value obtained by multiplying the polarity ("+" or "-") of data(n) or data(n-1) with a constant. For example, $\text{sign}(\text{data}(n-1)) \times 2$, which is obtained by multiplying the polarity of data(n-1) with a constant which is 2, may be the denominator of the equation (1). At this time, a phase error is calculated by the following equation (2).

[0078]

$$\text{Phase error} = [\text{data}(n) + \text{data}(n-1)] / [[\text{sign}(\text{data}(n-1)) \times 2] \dots (2)$$

30 [0079]

Provided that sign(a) is a function representing

the sign of "a", and when $a \geq 0$, $\text{sign}(a)=1$, and when $a < 0$, $\text{sign}(a)=-1$.

[0080]

Furthermore, for phase error detection, a phase
5 error detected by the phase error detecting section 41 of
Fig. 2 may be used, instead of that detected by the phase
error detecting section 51. In this case, the phase
error integrating section 41 supplies a phase error
signal to the bit slip correcting section 53, and the bit
10 slip correcting section 53 corrects an error caused by a
bit slip on the basis of the phase error signal supplied
from the phase error detecting section 41.

[0081]

Note that the phase error detecting section 51
15 detects a phase error signal on the basis of equalized
amplitude information and the corresponding reproduced
clock. By additionally using detected data outputted
from the data detecting section 35, a more accurate phase
error can be detected. This is because the detected data
20 outputted from the data detecting section 35 has its
error corrected, and this allows the phase error
detecting section 51 to detect the phase error between
the equalized amplitude information and the corresponding
reproduced clock by referring to the time at which the
25 polarities of the detected data thus error-corrected
switch.

[0082]

Moreover, a method of detecting a phase error in
the phase error detecting section 51 is not limited to
30 the method described with reference to Fig. 4, but may
include other schemes as well. For example, the phase

error detecting section 51 may classify equalized amplitude information, and detect a phase error on the basis of the classified equalized amplitude information.
[0083]

5 Fig. 5 is a timing chart showing detection of a deviation amount and detection of a time at which the deviation is predicted to have occurred, with respect to successive synchronization patterns, in a case where a bit slip has occurred.

10 [0084]

 "Synchronization pattern detection signal" is a signal outputted from the synchronization detecting section 52, and indicating that a synchronization pattern has been detected. That is, for example, a time at which
15 a synchronization pattern detection signal switches from 0 to 1 is a time at which a synchronization pattern has been detected.

[0085]

 "Normal synchronization pattern" represents a
20 normal synchronization pattern defined for each recording medium format. That is, an interval between normal synchronization patterns represents a predetermined period which is compared with an interval between synchronization pattern detection signals.

25 [0086]

 In the example of synchronization pattern detection signals and normal synchronization patterns shown in Fig. 5, on the left side of the figure, no bit slip has occurred in the preceding period, and thus a
30 synchronization pattern detection signal time coincides with a normal synchronization pattern time. By contrast,

on the right side of the figure, a bit slip has occurred in the preceding period, and thus the synchronization pattern detection signal deviates from the corresponding normal synchronization pattern. Note that, in a case where no bit slip occurs, a synchronization pattern detection signal is detected at a time at which a later-described synchronization counter value equals 19.

[0087]

"Predicted synchronization pattern range"

represents a range within which the detection range setting section 84 detects a synchronization pattern. For example, in a case of having detected a synchronization pattern from detected data within a period in which the predicted synchronization pattern range equals 1, the synchronization detecting section 52 switches a synchronization pattern detecting signal from 0 to 1, but in a case of having detected a synchronization pattern from detected data within a period in which the predicted synchronization pattern range equals 0, the synchronization detecting section 52 leaves the synchronization pattern detection signal unswitched.

[0088]

"Synchronization counter value" is a value counted by the synchronization pattern interval counter 91. For example, the synchronization pattern interval counter 91 sets the synchronization counter value to 0 when a synchronization pattern detection signal switches from 0 to 1 (including a predetermined delay), i.e., upon rise of the synchronization pattern detection signal. In an example shown in Fig. 5, there is a delay equal to one

cycle of the reproduced clock from the rise of a synchronization pattern detection signal to the setting of the synchronization counter value to 0. The synchronization pattern interval counter 91 increments the synchronization counter value in synchronism with a reproduced clock.

[0089]

In the example of the synchronization counter values shown in Fig. 5, when the synchronization counter value equals 18, the synchronization pattern detection signal has risen as shown on the right side of the figure, whereby the synchronization counter value switches from 18 to 0.

[0090]

"Phase error segment integrated value" is an integrated value of phase error values in each of segments obtained by dividing a normal synchronization pattern interval by a predetermined number. For example, in a case where one of the segments obtained by dividing the normal synchronization pattern interval by the predetermined number equals four cycles of the reproduced clock, the phase error integrating section 92 integrates phase error values in each segment corresponding to four cycles of the reproduced clock, whereby to calculate a phase error segment integrated value.

[0091]

In the example shown in Fig. 5, phase errors are integrated in each of segments obtained by dividing the normal synchronization pattern interval by 5. After the synchronization pattern detection signal has switched from 0 to 1, in a first segment which is the initial

segment, a phase error segment integrated value which is 0 is calculated, and in a second segment succeeding the first segment, a phase error segment integrated value which is -4 is calculated. Furthermore, in a third
5 segment succeeding the second segment, a phase error segment integrated value which is 2 is calculated, and in a fourth segment succeeding the third segment, a phase error segment integrated value which is -56 is calculated, and further in a fifth segment succeeding the fourth
10 segment, a phase error segment integrated value which is 38 is calculated.

[0092]

The absolute values of the phase error segment integrated values in the respective segments are
15 calculated by the bit slip judging section 81.

[0093]

In the example shown in Fig. 5, in the first segment, the absolute value of its phase error segment integrated value, which is 0, is calculated, and in the
20 second segment, the absolute value of its phase error segment integrated value, which is 4, is calculated. Furthermore, in the third segment, the absolute value of its phase error segment integrated value, which is 2, is calculated, and in the fourth segment, the absolute value
25 of its phase error segment integrated value, which is 56, is calculated, and further in the fifth segment, the absolute value of its phase error segment integrated value, which is 38, is calculated.

[0094]

30 Furthermore, maximum phase error segment integrated values in the respective segments are calculated by the

bit slip judging section 81.

[0095]

In the example shown in Fig. 5, in the first segment, the initial value 0 is compared with the absolute value of the phase error segment integrated value, which is 0, to calculate a maximum phase error segment integrated value resulting in 0. In the second segment, the maximum phase error segment integrated value in the first segment, which is 0, is compared with the absolute value of the phase error segment integrated value in the second segment, which is 4, to calculate a maximum phase error segment integrated value resulting in 4. Furthermore, in the third segment, the maximum phase error segment integrated value in the second segment, which is 4, is compared with the absolute value of the phase error segment integrated value in the third segment, which is 2, to calculate the maximum phase error segment integrated value resulting in 4, and in the fourth segment, the maximum phase error segment integrated value in the third segment, which is 4, is compared with the absolute value of the phase error segment integrated value in the fourth segment, which is 56, to calculate a maximum phase error segment integrated value resulting in 56. Moreover, in the fifth segment, the maximum phase error segment integrated value in the fourth segment, which is 56, is compared with the absolute value of the phase error segment integrated value in the fifth segment, which is 38, to calculate the maximum phase error segment integrated value resulting in 56.

30 [0096]

"Maximum phase error segment integrated value time"

is the heading synchronization counter value in a segment in which the absolute value of a phase error segment integrated value is selected as a maximum phase error segment integrated value. For example, in a case where
5 each of segments obtained by dividing a normal synchronization pattern interval by a predetermined number equals four cycles of the reproduced clock, the maximum phase error time storing section 93 stores the heading synchronization counter value in a segment having
10 the maximum phase error segment integrated value, as to the segments each corresponding to four cycles of the reproduced clock.

[0097]

Note that the maximum phase error segment
15 integrated value time is not limited to the heading synchronization counter value in a segment in which the absolute value of a phase error segment integrated value is selected as a maximum phase error segment integrated value, but may also include the last synchronization
20 counter value in the segment selected as having the maximum phase error segment integrated value, the median synchronization counter value in the segment selected as having the maximum phase error segment integrated value, or an arbitrary synchronization counter value in the
25 segment selected as having the maximum phase error segment integrated value.

[0098]

In the example shown in Fig. 5, in the first segment, the heading synchronization counter value in the
30 first segment having a maximum phase error segment integrated value is acquired, to store a maximum phase

error segment integrated value time which is 0 in the maximum phase error time storing section 93. In the second segment, the absolute value of its phase error segment integrated value is selected as a maximum phase error segment integrated value, and thus the heading synchronization counter value in the second segment is acquired, to store a maximum phase error segment integrated value time which is 4 in the maximum phase error time storing section 93.

10 [0099]

Furthermore, in the third segment, the absolute value of its phase error segment integrated value is not selected as a maximum phase error segment integrated value, and thus the maximum phase error segment integrated value time stored in the maximum phase error time storing section 93 remains unchanged. In the fourth segment, the absolute value of its phase error segment integrated value is selected as a maximum phase error segment integrated value, and thus the heading synchronization counter value in the fourth segment is acquired, to store a maximum phase error segment integrated value time which is 12 in the maximum phase error time storing section 93. And in the fifth segment, the absolute value of its phase error segment integrated value is not selected as a maximum phase error segment integrated value, and thus the maximum phase error segment integrated value time stored in the maximum phase error time storing section 93 remains unchanged.

[0100]

30 "Synchronization interval" equals the number of reproduced clocks between two successive synchronization

pattern detection signals. That is, the synchronization interval corresponds to a synchronization counter value at the rise of a synchronization pattern detection signal. In the example shown in Fig. 5, since the starting
 5 synchronization counter value is 0, the synchronization interval equals a value obtained by adding 1 to a synchronization counter value at the rise of a synchronization pattern detection signal.

[0101]

10 An interval between a synchronization pattern at a time n and a synchronization pattern at a time m will hereinafter be referred to as "synchronization pattern interval (n, m) ".

[0102]

15 In the example shown in Fig. 5, a synchronization interval which is 19 is calculated in a synchronization pattern interval $(k-1, k)$. Note that a synchronization interval which is 20 is calculated in a synchronization pattern interval $(k-2, k-1)$, and that a synchronization
 20 interval which is 20 is calculated in a synchronization pattern interval $(k, k+1)$.

[0103]

"Bit slip correction amount" is a difference between a period defined by synchronization pattern
 25 detection signals and a period defined by normal synchronization patterns, using reproduced clocks as a reference. In other words, it is a difference between a total synchronization counter value obtained in a normal synchronization pattern and a synchronization counter
 30 value immediately before the counter is reset by the rise of a synchronization pattern detection signal.

[0104]

That is, the bit slip correction amount represents a deviation between a reproduced clock and the corresponding equalized amplitude information, which has
5 been caused by a bit slip and which is measured using a cycle of the reproduced clock as a reference.

[0105]

In the example shown in Fig. 5, bit slip correction amounts are calculated as follows. In the
10 synchronization pattern interval $(k-1, k)$, i.e., at a time $k-1$, a bit slip correction amount which is 0 is calculated, and in the synchronization pattern interval $(k, k+1)$, the value 20 which is a normal synchronization interval is subtracted from a synchronization interval
15 which is 19, whereby to calculate a bit slip correction amount which is -1 at a time k .

[0106]

"Bit slip correction position" is a maximum phase error segment integrated value time stored in the maximum
20 phase error time storing section 93 upon rise of a synchronization pattern detection signal.

[0107]

That is, the bit slip correction position represents a time for a segment in which a deviation of
25 detected data (equalized amplitude information) is assumed to have occurred with respect to the corresponding reproduced clock.

[0108]

In the example shown in Fig. 5, bit slip correction
30 positions are calculated as follows. At the time $k-1$, a bit slip correction position which is 1 is calculated,

and at the time k , a bit slip correction position which is 12 is calculated.

[0109]

In the example shown in Fig. 5, in the
 5 synchronization pattern interval $(k, k+1)$, the bit slip correction amount which is -1 and the bit slip correction position which is 12 are supplied to the FIFO control section 82 as the bit slip correction information. Moreover, the bit slip judging section 81 judges that a
 10 bit slip has occurred since the bit slip correction amount, i.e., the deviation amount is other than 0.

[0110]

Note that in the synchronization pattern interval $(k-1, k)$, the bit slip correction amount equals 0 and the
 15 bit slip correction position equals 1. In this case, however, no bit slip correction is made, since the bit slip correction amount is 0, although the bit slip correction position takes a certain value.

[0111]

20 Fig. 6 is a diagram showing a method of calculating a bit slip occurrence position (a time for a segment in which a deviation of detected data (equalized amplitude information) is assumed to have occurred with respect to the corresponding reproduced clock), in a case where a
 25 bit slip has occurred.

[0112]

In Fig. 6, a mutual relationship is shown among
 "phase error segment integrated value", "detected data",
 "absolute value of phase error segment integrated value",
 30 "detected data after correction" and "detected data range for correction" in segments $N-1$, N and $N+1$ each defined

by synchronization pattern detection signals. Moreover, in an example shown in Fig. 6, a bit slip has occurred at a time A.

[0113]

5 A waveform 211 represents integrated values of phase errors, calculated by the phase error integrating section 92. Rectangles shown in a manner overlapping with the waveform 211 respectively represent integrated values of phase errors in segments.

10 [0114]

 The detected data is detected by the data detecting section 35. In the example shown in Fig. 6, L channel bit detected data is arranged between two normal synchronization patterns in a case where no bit slip occurs. In a case where a bit slip has occurred, detected data either above or below L is arranged between two synchronization patterns.

[0115]

 In the example shown in Fig. 6, a bit slip has occurred in the segment N, and thus detected data in the segment N equals (L+1) channel bits.

[0116]

 Since the absolute value of a phase error segment integrated value is an absolute value as to a phase error segment integrated value, a phase error segment integrated value which is a negative value becomes a positive value with its sign inverted. Furthermore, through a comparison among the absolute values of phase error segment integrated values, the absolute value of a phase error segment integrated value in a segment denoted by B becomes the maximum phase error segment integrated

value, and thus (a time for) the segment denoted by B becomes the bit slip correction position.

[0117]

The detected data is corrected into data having as many detected data bits as those to be arranged between two normal synchronization patterns in a case where no bit slip occurs. In the example shown in Fig. 6, the "detected data after correction" is corrected so as to have L channel bits.

10 [0118]

As a result of this correction, the detected data from the time for the segment denoted by B to the end of the segment N are corrected. In segments 212 with large phase errors, the reproduced signals themselves have changed, and thus, even if a correction is made in the time direction, normal detected data cannot be obtained. In segments 213 with small phase errors, the reproduced signals themselves have recovered, and thus normal detected data can be obtained by a correction in the time direction.

20 direction.

[0119]

In this way, in a case where a burst error has occurred and a bit slip has occurred due to the burst error, the reproducing apparatus of the present invention can correct an error preceding a synchronization pattern which is detected after the bit slip.

25 which is detected after the bit slip.

[0120]

Next, insertion of a synchronization pattern detection signal will be described. Once a burst error has occurred, detection of a synchronization pattern itself may become difficult in some cases. In a case

30 has occurred, detection of a synchronization pattern itself may become difficult in some cases. In a case

where synchronization patterns have been detected successively in a predetermined period, the reproducing apparatus moves to a synchronization pattern interpolation mode, to insert a synchronization pattern detection signal at a predetermined time.

[0121]

Fig. 7 is a timing chart for explaining insertion of a synchronization pattern detection signal in a case where no synchronization pattern has been detected in the synchronization pattern interpolation mode.

[0122]

"Synchronization pattern detection signal" to "reproduced clock", and "synchronization counter value" to "bit slip correction position" in Fig. 7 are similar to those in the case shown in Fig. 5, and thus their description will be omitted whenever appropriate.

[0123]

In an example shown in Fig. 7, a synchronization pattern at a time k is not detected, and thus no synchronization pattern detection signal rises at the time k . A mark "x" in Fig. 7 indicates that a synchronization pattern detection signal does not rise.

[0124]

In the synchronization pattern interpolation mode, in a case where no synchronization pattern is detected from detected data during a period in which the predicted synchronization pattern range equals 1, the synchronization pattern detection signal inserting section 85 inserts a synchronization pattern detection signal into the middle of the predicted synchronization pattern range set by the detection range setting section

84, i.e., at a time coinciding with a normal synchronization pattern.

[0125]

Note that the synchronization detecting section 52
5 to the bit slip correcting section 53 need a predetermined delay time for their signal processing. Thus, the synchronization pattern detection signal inserting section 85 inserts a synchronization pattern detection signal with the corresponding signals keeping
10 time relations to one another by utilizing that delay time.

[0126]

A "synchronization pattern detection signal after interpolation" shown in Fig. 7 represents the
15 synchronization pattern detection signal which has been inserted at the time k.

[0127]

Here, a procedure for inserting a synchronization pattern will be described. The synchronization detecting
20 section 52 first finds a synchronization pattern itself from detected data (hereinafter referred to as "synchronization pattern interpolation release mode"). In a case where at least one synchronization pattern has been detected, if a next synchronization pattern is found
25 "within margins on both sides of" a regular clock count, i.e., within a predetermined range, in accordance with a recording medium format, it is determined whether or not the synchronization pattern is valid by multiplication of the occurring probabilities of both the synchronization
30 pattern and its synchronization pattern position (time). And in a case where the synchronization pattern is

determined to be valid, a next synchronization pattern is found using that synchronization pattern position (time) as a reference. The term "within margins on both sides of" is generally referred to as a "detection window", and
5 is used to allow for some deviation from regular clocks (normal interval) in a synchronization pattern interval, e.g., where a bit slip has occurred at some point along the processing.

[0128]

10 And in a case where synchronization patterns have been found as many as N times ("N" is a set value defined by an actual circuit or the specification of a product) in succession, if, after narrowing the detection window to some extent, no synchronization pattern is found in
15 that detection window, the synchronization detecting section 52 inserts a synchronization pattern (actually, a synchronization pattern detection signal) into the middle of the window, and thereafter continues the synchronization pattern detection (i.e., moves to the
20 synchronization pattern interpolation mode). However, in a case where no synchronization pattern has been found as many as M times ("M" is a set value defined by the actual circuit or the specification of the product) in succession, the synchronization detecting section 52
25 returns to the synchronization pattern interpolation release mode.

[0129]

In the example shown in Fig. 7, the reproducing apparatus is in the synchronization pattern interpolation
30 mode, and thus a synchronization pattern detection signal is inserted at the time k.

[0130]

In the example shown in Fig. 7, phase error segment integrated values are obtained as follows. In segments obtained by dividing a "synchronization pattern interval after interpolation" (k-1, k) by 5, phase errors are
 5 integrated, and in segments obtained by dividing a "synchronization pattern interval after interpolation" (k, k+1) by 6, phase errors are integrated.

[0131]

10 After a "synchronization pattern detection signal after interpolation" has switched from 0 to 1 in the "synchronization pattern interval after interpolation" (k-1, k), a phase error segment integrated value which is 0 is calculated in a first segment which is the initial
 15 segment, and a phase error segment integrated value which is -1 is calculated in a second segment succeeding the first segment. Furthermore, a phase error segment integrated value which is 1 is calculated in a third segment succeeding the second segment, a phase error
 20 segment integrated value which is -8 is calculated in a fourth segment succeeding the third segment, and a phase error segment integrated value which is 5 is calculated in a fifth segment succeeding the fourth segment.

[0132]

25 Furthermore, after a "synchronization pattern detection signal after interpolation" has switched from 0 to 1 in the "synchronization pattern interval after interpolation" (k, k+1), in a first segment which is the initial segment, a phase error segment integrated value
 30 which is -3 is calculated, and in a second segment succeeding the first segment, a phase error segment

integrated value which is 2 is calculated. Furthermore,
 a phase error segment integrated value which is 1 is
 calculated in a third segment succeeding the second
 segment, a phase error segment integrated value which is
 5 -1 is calculated in a fourth segment succeeding the third
 segment, and a phase error segment integrated value which
 is 1 is calculated in a fifth segment succeeding the
 fourth segment. Moreover, due to a bit slip having
 occurred, in a sixth segment succeeding the fifth segment,
 10 a phase error integrated value which is 0 is calculated.
 [0133]

As the absolute values of the phase error segment
 integrated values, in the synchronization pattern
 interval $(k-1, k)$ in the example shown in Fig. 7, the
 15 absolute value of its phase error segment integrated
 value, which is 0, is calculated in the first segment,
 and the absolute value of its phase error segment
 integrated value, which is 1, is calculated in the second
 segment. Furthermore, the absolute value of its phase
 20 error segment integrated value, which is 1, is calculated
 in the third segment, the absolute value of its phase
 error segment integrated value, which is 8, is calculated
 in the fourth segment, and the absolute value of its
 phase error segment integrated value, which is 5, is
 25 calculated in the fifth segment.
 [0134]

Furthermore, in the synchronization pattern
 interval $(k, k+1)$, the absolute value of its phase error
 segment integrated value, which is 3, is calculated in
 30 the first segment, the absolute value of its phase error
 segment integrated value, which is 2, is calculated in

the second segment, and the absolute value of its phase error segment integrated value, which is 1, is calculated in the third segment. And the absolute value of its phase error segment integrated value, which is 1, is calculated in the fourth segment, the absolute value of its phase error segment integrated value, which is 1, is calculated in the fifth segment, and the absolute value of its phase error segment integrated value, which is 0, is calculated in the sixth segment.

10 [0135]

As maximum phase error segment integrated values, in the synchronization pattern interval $(k-1, k)$ in the example shown in Fig. 7, the initial value 0 is compared with the absolute value of its phase error segment integrated value, which is 0, to calculate a maximum phase error segment integrated value which is 0 in the first segment. In the second segment, the maximum phase error segment integrated value in the first segment, which is 0, is compared with the absolute value of the phase error segment integrated value in the second segment, which is 1, to calculate a maximum phase error segment integrated value which is 1. Furthermore, in the third segment, the maximum phase error segment integrated value in the second segment, which is 1, is compared with the absolute value of the phase error segment integrated value in the third segment, which is 1, to calculate the maximum phase error segment integrated value which is 1, and in the fourth segment, the maximum phase error segment integrated value in the third segment, which is 1, is compared with the absolute value of the phase error segment integrated value in the fourth segment, which is

8, to calculate a maximum phase error segment integrated value which is 8. Moreover, in the fifth segment, the maximum phase error segment integrated value in the fourth segment, which is 8, is compared with the absolute value of the phase error segment integrated value in the fifth segment, which is 5, to calculate the maximum phase error segment integrated value which is 8.

[0136]

Furthermore, in the synchronization pattern interval $(k, k+1)$, the initial value 0 is compared with the absolute value of its phase error segment integrated value, which is 3, to calculate a maximum phase error segment integrated value which is 3 in the first segment. In the second segment, the maximum phase error segment integrated value in the first segment, which is 3, is compared with the absolute value of the phase error segment integrated value in the second segment, which is 2, to calculate the maximum phase error segment integrated value which is 3. Furthermore, in the third segment, the maximum phase error segment integrated value in the second segment, which is 3, is compared with the absolute value of the phase error segment integrated value in the third segment, which is 1, to calculate the maximum phase error segment integrated value which is 3, and in the fourth segment, the maximum phase error segment integrated value in the third segment, which is 3, is compared with the absolute value of the phase error segment integrated value in the fourth segment, which is 1, to calculate the maximum phase error segment integrated value, which is 3.

[0137]

Moreover, in the fifth segment, the maximum phase error segment integrated value in the fourth segment, which is 3, is compared with the absolute value of the phase error segment integrated value in the fifth segment, which is 1, to calculate the maximum phase error segment integrated value which is 3, and in the sixth segment, the maximum phase error segment integrated value in the fifth segment, which is 3, is compared with the absolute value of the phase error segment integrated value in the sixth segment, which is 0, to calculate the maximum phase error segment integrated value which is 3.

[0138]

In the synchronization pattern interval $(k-1, k)$ in the example shown in Fig. 7, as maximum phase error segment integrated value times, in the example shown in Fig. 7, the heading synchronization counter value in the first segment having a maximum phase error segment integrated value is acquired, to store a maximum phase error segment integrated value time which is 0 in the maximum phase error time storing section 93 in the first segment. In the second segment, the absolute value of a phase error segment integrated value error is selected as a maximum phase error segment integrated value, and thus the heading synchronization counter value in the second segment is acquired, to store a maximum phase error segment integrated value time which is 4 in the maximum phase error time storing section.

[0139]

Furthermore, in the third segment, the absolute value of a phase error segment integrated value error is selected as a maximum phase error segment integrated

value, and thus the heading synchronization counter value in the third segment having the maximum phase error segment integrated value is acquired, to store a maximum phase error segment integrated value time which is 8 in
 5 the maximum phase error time storing section. In the fourth segment, the absolute value of a phase error segment integrated value error is selected as a maximum phase error segment integrated value, and thus the heading synchronization counter value in the fourth
 10 segment having the maximum phase error segment integrated value is acquired, to store a maximum phase error segment integrated value time which is 12 in the maximum phase error time storing section. And in the fifth segment, the absolute value of a phase error segment integrated
 15 value error is not selected as a maximum phase error segment integrated value, and thus the maximum phase error segment integrated value time stored in the maximum phase error time storing section 93 remains unchanged.

[0140]

20 Furthermore, in the synchronization pattern interval $(k, k+1)$ in the example shown in Fig. 7, as maximum phase error segment integrated value times, in the first segment, the heading synchronization counter value in the first segment having a maximum phase error
 25 segment integrated value is acquired, to store a maximum phase error segment integrated value time which is 0 in the maximum phase error time storing section 93. In the second segment, the absolute value of a phase error segment integrated value error is not selected as a
 30 maximum phase error segment integrated value, and thus the maximum phase error segment integrated value time

stored in the maximum phase error time storing section 93 remains unchanged. In the third segment, the absolute value of a phase error segment integrated value error is not selected as a maximum phase error segment integrated value, and thus the maximum phase error segment integrated value time stored in the maximum phase error time storing section 93 remains unchanged.

[0141]

In the fourth segment, the absolute value of a phase error segment integrated value error is not selected as a maximum phase error segment integrated value, and thus the maximum phase error segment integrated value time stored in the maximum phase error time storing section 93 remains unchanged. In the fifth segment, the absolute value of a phase error segment integrated value error is not selected as a maximum phase error segment integrated value, and thus the maximum phase error segment integrated value time stored in the maximum phase error time storing section 93 remains unchanged. And in the sixth segment, the absolute value of a phase error segment integrated value error is not selected as a maximum phase error segment integrated value, and thus the maximum phase error segment integrated value time stored in the maximum phase error time storing section 93 remains unchanged.

[0142]

Note that in a case where maximum phase error segment integrated values are equal in successive segments, which one of the former and latter maximum phase error segment integrated values should prevail is determined by setting. In the example shown in Fig. 7,

the maximum phase error segment integrated values in the second and third segments are 1, and the maximum phase error segment integrated value time in the third segment is 8. Here, if the maximum phase error segment

5 integrated values are equal, it is set such that the latter maximum phase error segment integrated value should prevail, and thus the value in the third segment prevails over that in the second segment.

[0143]

10 In the example shown in Fig. 7, synchronization intervals are calculated as follows: a synchronization interval which is 20 is calculated in the "synchronization pattern interval after correction" ($k-1$, k), a synchronization interval which is 20 is calculated
15 in the "synchronization pattern interval after correction" (k , $k+1$), and a synchronization interval which is 21 is calculated in a "synchronization pattern interval after correction" ($k+1$, $k+2$).

[0144]

20 In the example shown in Fig. 7, bit slip correction amounts are calculated as follows: a bit slip correction amount which is 0 is calculated in the "synchronization pattern interval after correction" ($k-1$, k), i.e., at the time $k-1$, and a bit slip correction amount which is 0 is
25 calculated in the "synchronization pattern interval after correction" (k , $k+1$), i.e., at the time k . Moreover, in the "synchronization pattern interval after correction" ($k+1$, $k+2$), i.e., at a time $k+1$, a bit slip correction amount which is 1 is calculated.

30 [0145]

Here, for example, at the time k , the

synchronization pattern detection signal inserting
 section 85 inserts the synchronization pattern detection
 signal at the predetermined time, and thus 0 is
 calculated as the bit slip correction amount at the time
 5 k.

[0146]

In the example shown in Fig. 7, bit slip correction
 positions are calculated as follows: a bit slip
 correction position which is 0 is calculated at the time
 10 k-1, a bit slip correction position which is 12 is
 calculated at the time k, and a bit slip correction
 position which is 0 is calculated at the time k+1.

[0147]

In a case where the synchronization pattern
 15 detection signal inserting section 85 has inserted a
 synchronization pattern detection signal at a
 predetermined time, a bit slip correction is made at a
 time at which a first synchronization pattern detection
 signal is detected after the synchronization pattern
 20 detection signal has been inserted. In the example shown
 in Fig. 7, at the time k+1, which is after the time k at
 which the synchronization pattern detection signal has
 been inserted, a bit slip correction is made. And the
 bit slip correction amount which is 1 and the bit slip
 25 correction position which is 12 are supplied to the FIFO
 control section 82 as the bit slip correction information.
 In this case, the bit slip judging section 81 judges that
 a bit slip has occurred because the bit slip correction
 amount, i.e., the deviation amount is other than 0.

30 [0148]

Note that at the time k, the bit slip correction

amount equals 0 and the bit slip correction position equals 12. In this case, however, no bit slip correction is made, since the bit slip correction amount is 0, although the bit slip correction position takes a certain value.

[0149]

Fig. 8 is a diagram showing a method of calculating a bit slip occurrence position in a case where a bit slip has occurred and no synchronization pattern has been detected.

[0150]

In Fig. 8, a mutual relationship is shown among "phase error segment integrated value", "detected data", "absolute value of phase error segment integrated value", "detected data after correction" and "detected data range for correction" in segments N-1, N and N+1 each defined by synchronization pattern detection signals.

[0151]

"Phase error segment integrated value" to "detected data range for correction" in Fig. 8 are similar to those in the case shown in Fig. 6, and thus their description will be omitted whenever appropriate.

[0152]

Similarly to the case shown in Fig. 6, rectangles shown in a manner overlapping with a waveform 211 respectively represent phase error segment integrated values. That is, in an example shown in Fig. 8, a synchronization pattern detection signal is inserted at a time at which the segment N switches to the segment N+1, and the rectangles shown so as to overlap with the waveform 211 respectively represent phase error

integrated values in segments, in the segment N+1 after the synchronization pattern detection signal has been inserted.

[0153]

5 As to "detected data", in the example shown in Fig. 8, detected data of L channel bit is arranged in the segment N-1 in which no bit slip has occurred. Moreover, in the segments N and N+1, a bit slip has occurred, and thus no synchronization pattern has been detected.

10 Consequently, through the segments N and N+1, detected data of (L+L+1) channel bit is arranged.

[0154]

 In the example shown in Fig. 8, in the segment N+1 after the synchronization pattern detection signal has

15 been inserted, the absolute value of a phase error segment integrated value in a segment C becomes maximum, and thus (a time for) the segment denoted by C is the bit slip correction position.

[0155]

20 As to "detected data after interpolation", in the example shown in Fig. 8, in the segment N in which no bit slip is deemed to have occurred, detected data of L channel bit is arranged. In other words, since the synchronization pattern detection signal is inserted,

25 detected data of L channel bit is arranged in the segment N, and the remaining detected data of (L+1) channel bit is arranged in the segment N+1.

[0156]

 Then, in the segment N+1, the detected data of

30 (L+1) channel bit is changed to data of L channel bit by correction.

[0157]

That is, bit slip correction is executed such that the detected data in the segment N+1 equals L channel bits.

5 [0158]

As to "detection data range for correction", the reproduced signals themselves have changed in segments 221, and thus, even if a correction is made in the time direction, normal detected data cannot be obtained.

10 Since the reproduced signals themselves have recovered in segments 222, normal detected data can be detected by making a correction in the time direction.

[0159]

Thus, in a case where no synchronization pattern
15 has been detected, the invention apparatus of the present invention inserts a synchronization pattern detection signal at a predetermined time, to supplement a synchronization pattern, whereby an error preceding the synchronization pattern which is detected after a bit
20 slip can be corrected.

[0160]

Referring to flowcharts of Figs. 9 to 13, processing will be described, which is performed by the reproducing apparatus that executes a correction program
25 by using phase errors.

[0161]

Fig. 9 is a flowchart for explaining a reproduction process by the reproducing apparatus.

[0162]

30 In step S1, the equalizer 31 shapes a reproduced signal reproduced by a pickup, not shown, from a

recording medium, such as an optical disc, a hard disk or a digital video cassette, which is attached, and supplies the reproduced signal to the A/D converting section 32.

[0163]

5 In step S2, the A/D converting section 32 converts the reproduced signal, which is an analog signal supplied from the equalizer 31, into digital signals on the basis of reproduced clocks to be supplied from the clock generating section 33. The A/D converting section 32
10 supplies the digital signals generated by the conversion, to the clock generating section 33 and the equalizer 34.

[0164]

 In step S3, the clock generating section 33 includes the phase error detecting section 41 and the VCO
15 42, and generates the reproduced clocks from the digital signals using the PLL system.

[0165]

 In step S4, the equalizer 34 adjusts the edge position of each digital signal in the time direction on
20 the basis of the reproduced clock, to shape the digital signal, and supplies the shaped digital signal to the data detecting section 35 and the error correcting section 36.

[0166]

25 In step S5, the data detecting section 35 corrects the digital signal error by means of Viterbi decoding, and generates the error-corrected digital signal as detected data. Note that the data detecting section 35 may alternatively utilize a maximum-likelihood decoding
30 system other than Viterbi decoding.

[0167]

In step S6, a bit slip correcting process is executed, and then the process returns to step S1 to repeat the above-mentioned processing.

[0168]

5 Details of the bit slip correcting process in step S6 will be described with reference to the flowchart of Fig. 10.

[0169]

10 In step S21, the synchronization detecting section 52 executes a synchronization pattern detecting process.

[0170]

15 Details of the synchronization pattern detecting process in the synchronization pattern interpolation mode, which corresponds to step S21, will be described with reference to the flowchart of Fig. 11.

[0171]

20 In step S31, the synchronization detecting section 52 detects a synchronization pattern. For example, the synchronization detecting section 52 detects a synchronization pattern which has a specific bit arrangement defined by a recording medium format and which is contained in the detected data.

[0172]

25 In step S32, the detection range setting section 84 sets a detection range from which a synchronization pattern is to be detected, on the basis of a reproduced clock signal count, and determines whether or not a synchronization pattern has been detected within the detection range. If it is determined in step S32 that no
30 synchronization pattern has been detected, the process proceeds to step S33, in which the synchronization

pattern detection signal inserting section 85
interpolates a synchronization pattern, after which the
process is terminated. For example, in step S33, the
synchronization pattern detection signal inserting
5 section 85 inserts a synchronization pattern at a
predetermined period (at a time coinciding with a normal
synchronization pattern).

[0173]

If it is determined in step S32 that a
10 synchronization pattern has been detected within the
detection range, there is no need to interpolate a
synchronization pattern, and thus, the process is
terminated by skipping the process of step S33.

[0174]

15 Returning to Fig. 10, in step S22, the phase error
detecting section 51 detects a phase error between
equalized amplitude information supplied from the
equalizer 34 and the corresponding reproduced clock, and
supplies a phase error signal representing the phase
20 error, to the bit slip correcting section 53.

[0175]

In step S23, the bit slip correcting section 53
detects a difference between the sync signal detected by
the synchronization detecting section 52 and the
25 predetermined period as the deviation amount, on the
basis of the corresponding reproduced clocks.

[0176]

In step S24, the bit slip correcting section 53
executes a correction information calculating process.

30 [0177]

Details of the correction information calculating

process in step S24 will be described with reference to the flowchart of Fig. 12.

[0178]

In step S41, the phase error integrating section 92
5 integrates phase errors detected in each of predetermined segments, to calculate a phase error segment integrated value.

[0179]

In step S42, the bit slip judging section 81
10 detects a maximum for the absolute values of the phase error segment integrated values.

[0180]

In step S43, the maximum phase error time storing section 93 detects a bit slip correction position which
15 is a time at which the absolute value of the phase error segment integrated value, which is maximum, has been detected, after which the process is terminated.

[0181]

Returning to Fig. 10 again, in step S25, the bit
20 slip correcting section 53 executes a FIFO control process, after which the bit slip correcting process is terminated.

[0182]

Details of the FIFO control process in step S25
25 will be described with reference to the flowchart of Fig. 13.

[0183]

In step S51, the FIFO control section 82 acquires the bit slip correction amount representing a deviation
30 amount, and the bit slip correction position representing a deviation occurrence time, from the bit slip judging

section 81.

[0184]

In step S52, in a case where a deviation amount which is other than 0 has been detected, the FIFO control section 82 supplies a control signal for controlling the FIFO buffer 83 to move data of interest in the time direction so as to correspond to the deviation amount, to the FIFO buffer 83, whereby to control writing and reading by the FIFO buffer 83. The FIFO buffer 83 moves the detected data in the time direction so as to correspond to the deviation amount on the basis of the control information supplied from the FIFO control section 82, to make a detected data correction corresponding to the bit slip and then output the corrected detected data, after which the process is terminated.

[0185]

Referring to Figs. 14 to 17, detected data correction performed in step S52 by the FIFO buffer 83 will be described.

[0186]

Fig. 14 is a diagram for explaining detected data correction in the FIFO buffer 83 that is controlled to increase the number of detected data bits, in a case where a bit slip correction amount is below 0.

[0187]

The FIFO buffer 83 is controlled by a RE (Read Enable) signal, and a WE (Write Enable) signal supplied from the FIFO control section 82 on the basis of the bit slip correction information. In a case where the RE signal is "ON" (e.g., 1), the FIFO buffer 83 sequentially

outputs detected data it stores in synchronism with reproduced clocks, and in a case where the RE signal is "OFF" (e.g., 0), it repeatedly outputs the same detected data in synchronism with reproduced clocks.

5 [0188]

Moreover, in a case where the WE signal is "ON" (e.g., 1), the FIFO buffer 83 sequentially stores detected data supplied from the data detecting section 35 in synchronism with reproduced clocks, and in a case
10 where the WE signal is "OFF" (e.g., 0), it stores detected data supplied from the data detecting section 35 such that a detected data bit stored one reproduced clock ahead is overwritten, in synchronism with a reproduced clock.

15 [0189]

In Figs. 14 to 17, each of rectangles denoted by characters A to E represents one channel bit contained in the corresponding detected data.

[0190]

20 As shown on the left side of Fig. 14, an example will be described in which a channel bit which is A, a channel bit which is B, a channel bit which is C, a channel bit which is D and a channel bit which is E are sequentially supplied from the data detecting section 35
25 to the FIFO buffer 83.

[0191]

The FIFO buffer 83 sequentially stores the channel bits A to E supplied during a period in which the WE signal is "ON".

30 [0192]

The FIFO buffer 83 outputs the channel bits A to E

stored in a sequence, in that sequence, in synchronism with reproduced clocks, during a period in which the RE signal is "ON".

[0193]

5 In an example shown in Fig. 14, the FIFO buffer 83 keeps the WE signal in the "ON" state at all times for the detected data bits A to E supplied. At a time for reading the data bit C, the FIFO buffer 83 puts the RE signal to "OFF" whereby the FIFO buffer 83 outputs the
10 channel bit A, the channel bit B, the channel bit C, the channel bit C, the channel bit D and the channel bit E.

[0194]

Fig. 15 is a timing chart showing data control in the FIFO buffer 83 to increase detected data.

15 [0195]

In an example shown in Fig. 15, "detected data supplied" corresponds to a data arrangement on the left side of Fig. 14. In the example shown in Fig. 15, the detected data, which are the channel bit A, the channel
20 bit B, the channel bit C, the channel bit D and the channel bit E, are sequentially supplied to the FIFO buffer 83.

[0196]

The WE signal is a write control signal supplied
25 from the FIFO control section 82 to the FIFO buffer 83. Where the WE signal is "ON", the FIFO buffer 83 advances a WritePointer in synchronism with a reproduced clock to store a channel bit contained in the detected data supplied, and where the WE signal is "OFF", it stores a
30 channel bit contained in the detected data supplied without causing the WritePointer to advance.

[0197]

In the example shown in Fig. 15, since the WE signal stays "ON" at all times, the FIFO buffer 83 stores the supplied detected data in such a sequence as detected.

5 [0198]

"Detected data stored" in the figure is detected data stored in the FIFO buffer 83. The detected data supplied, i.e., the channel bit A, the channel bit B, the channel bit C, the channel bit D and the channel bit E
10 are sequentially stored.

[0199]

Note that each of the stored detected data in the figure is one reproduced clock behind the corresponding one of the supplied detected data. This means that the
15 process of storing detected data is executed one clock behind.

[0200]

The RE signal is read control information supplied from the FIFO control section 82 to the FIFO buffer 83.
20 In a case where the RE signal is "ON", the FIFO buffer 83 advances a ReadPointer in synchronism with a reproduced clock, and outputs a channel bit specified by the ReadPointer. In a case where the RE signal is "OFF", it outputs a channel bit specified by the ReadPointer
25 without causing the ReadPointer to advance.

[0201]

In the example shown in Fig. 15, to read the channel bit A or B, the RE signal is set to "ON", and to read the channel bit C, it is set to "OFF". Furthermore,
30 to read the channel bit D or E, the RE signal is set to "ON".

[0202]

Therefore, the FIFO buffer 83 does not cause the ReadPointer to advance after having read the channel bit C, and thus it reads the channel bit C twice, whereby to
5 increase the number of detected data bits for output, by 1, compared with the detected data bits supplied.

[0203]

In the example shown in Fig. 15, detected data, which are the channel bit A, the channel bit B, the
10 channel bit C, the channel bit C, the channel bit D and the channel bit E, are sequentially outputted.

[0204]

Note that the detected data outputted deviate one reproduced clock in the time direction from the detected
15 data stored. This means that output of detected data is executed one clock behind.

[0205]

Fig. 16 is a diagram for explaining detected data correction in the FIFO buffer 83 that is controlled to
20 decrease the number of detected data bits, in a case where a bit slip correction amount exceeds 0.

[0206]

A detected data correcting process in Fig. 16 which is performed by the FIFO buffer 83 is similar to that in
25 the case shown in Fig. 14, and thus its description will be omitted whenever appropriate.

[0207]

As shown on the left side of Fig. 16, a channel bit A, a channel bit B, a channel bit C, a channel bit D and
30 a channel bit E are supplied to the FIFO buffer 83 sequentially.

[0208]

In an example shown in Fig. 16, a WE signal is set to "OFF" at a time at which the channel bit C is to be stored. If the RE signal is "OFF", the FIFO buffer 83
 5 overwrites a detected data bit stored one clock ahead with a detected data bit next thereto. Thus, the channel bit C is overwritten with the channel bit D, whereby to store the channel bit A, the channel bit B, the channel bit D and the channel bit E sequentially.

10 [0209]

The FIFO buffer 83 outputs the channel bit A, the channel bit B, the channel bit D and the channel bit E in this sequence.

[0210]

15 Fig. 17 is a timing chart showing data control by the FIFO buffer 83 to decrease detected data.

[0211]

"Reproduced clock" to "detection data for output" in Fig. 17 are similar to those in the case shown in Fig.
 20 15, and thus their description will be omitted whenever appropriate.

[0212]

In an example shown in Fig. 17, the WE signal is set to "ON" in a case where the channel bit A or B is
 25 supplied, and to "OFF" in a case where the channel bit C is supplied. Furthermore, the WE signal is set to "ON" in a case where the channel bit D or E is supplied.

[0213]

Therefore, in this case, the FIFO buffer 83 stops
 30 the WritePointer after having written the channel bit C to overwrite the channel bit C with the channel bit D,

whereby to decrease the number of detected data bits for storage, by 1.

[0214]

That is, the FIFO buffer 83 stores the channel bit
5 A, the channel bit B, the channel bit D and the channel
bit E sequentially.

[0215]

In the example shown in Fig. 17, the RE signal
stays "ON" at all times, and thus the FIFO buffer 83
10 outputs the stored detected data sequentially.

[0216]

The FIFO buffer 83 outputs the channel bit A, the
channel bit B, the channel bit D and the channel bit E
sequentially.

15 [0217]

Note that the FIFO buffer 83 may include, not only
a FIFO buffer, but also a general-type memory. For
example, in a case where detected data is to be increased
in a memory with general addressing, a circuit may be
20 configured such that an address for writing into the
memory is incremented by 1 with respect to a reproduced
clock at all times, and such that an address for reading
from the memory is stopped at any location where
operation should be performed or is put back by a
25 necessary amount. Moreover, in a case where detected
data is to be decreased, the circuit may be configured
such that an address for writing into the memory is
stopped at any location where operation should be
performed or is put back by a necessary amount, and such
30 that an address for reading from the memory is
incremented by 1 with respect to a reproduced clock at

all times.

[0218]

A circuit configuration in a case where a general memory is used is similar to the circuit configuration in
5 a case where a FIFO buffer is used.

[0219]

Referring next to Figs. 18 to 27, an embodiment of the present invention will be described, in a case where bit slip correction is to be performed using errors
10 (hereinafter referred to as "zero-crossing offsets") in an amplitude direction of two successive equalized amplitude information bits having different polarities (signs).

[0220]

15 Fig. 18 is a block diagram showing another configuration of an embodiment of the reproducing apparatus according to the present invention. Portions similar to those in the case shown in Fig. 2 are denoted by the same reference numerals, and their description
20 will be omitted whenever appropriate.

[0221]

An error correcting section 36 includes a zero-crossing offset detecting section 301, a synchronization detecting section 52 and a bit slip correcting section
25 302. That is, the error correcting section 36 may include the zero-crossing offset detecting section 301 and the bit slip correcting section 302, instead of the phase error detecting section 51 and the bit slip correcting section 53 described with reference to Fig. 2.

30 [0222]

The zero-crossing offset detecting section 301

detects a zero-crossing offset on the basis of equalized amplitude information supplied from an equalizer 34 and a reproduced clock supplied from a clock generating section 33, and supplies a zero-crossing offset signal

5 representing the zero-crossing offset, to the bit slip correcting section 302.

[0223]

Fig. 19 is a block diagram showing details of the synchronization detecting section and the bit slip
10 correcting section. Portions similar to those in the case shown in Fig. 3 are denoted by the same reference numerals, and their description will be omitted whenever appropriate.

[0224]

15 A bit slip judging section 311 includes a synchronization pattern interval counter 91, a zero-crossing offset integrating section 321 and a maximum zero-crossing offset time storing section 322. That is, the bit slip judging section 311 may include the zero-
20 crossing offset integrating section 321 and the maximum zero-crossing offset time storing section 322, instead of the phase error integrating section 92 and the maximum phase error time storing section 93 described with reference to Fig. 3.

25 [0225]

The zero-crossing offset integrating section 321 integrates zero-crossing offsets detected in each of segments into which an interval between two successive synchronization patterns is divided, whereby to calculate
30 a zero-crossing offset segment integrated value. Here, a segment into which the interval is divided is determined

by any of the predetermined number of zero-crossing offsets, a predetermined period and predetermined channel bits.

[0226]

5 The maximum zero-crossing offset time storing section 322 detects a time at which a deviation between a reproduced clock and equalized amplitude information is predicted to have occurred, which is a time defining a segment in which the absolute value of an integrated
10 value obtained by integration becomes maximum between two successive synchronization patterns, and stores that time.

[0227]

Referring next to Fig. 20, an example of zero-crossing offset detection in the zero-crossing offset
15 detecting section 301 will be described.

[0228]

Fig. 20 is a diagram showing the signal waveform of reproduced clocks, detected data which can take either "1" or "0", and values of equalized amplitude information,
20 with a time axis t extending in the horizontal direction. In Fig. 20, $\text{data}(n-1)$ and $\text{data}(n)$ are amplitude values of the equalized amplitude information at the rises of reproduced clocks, respectively. The " $\text{data}(n)$ " is an amplitude value of the equalized amplitude information
25 next to the " $\text{data}(n-1)$ ".

[0229]

A zero-crossing offset is calculated by, e.g., the following equation (3).

[0230]

30 Zero-crossing offset = $[\text{data}(n) + \text{data}(n-1)]/2 \dots$
(3)

[0231]

From the equation (3), an offset amount between two successive equalized amplitude information bits having different polarities (signs) is calculated.

5 [0232]

Note that in the equation (3), its denominator can be set to an arbitrary integer other than 0. In this case, e.g., 1 may be set, instead of 2.

[0233]

10 An offset between two successive equalized amplitude information bits having different polarities (signs) is a zero-crossing offset. The arrow in Fig. 20 represents a zero-crossing offset.

[0234]

15 In a case where an error is contained in equalized amplitude information, in a coordinate space having time and amplitude value of equalized amplitude information as its coordinate axes, respectively, a straight line connecting a point specified by the start time of a
20 certain cycle of the reproduced clock and the amplitude value data(n-1) of the equalized amplitude information at that start time, with a point specified by the start time of the next cycle of the reproduced clock and the amplitude value data(n) of the equalized amplitude
25 information at the start time of the next cycle does not pass through a point specified by the half cycle point and an amplitude value which is 0. In a case where an error is contained in the equalized amplitude information, this straight line deviates from the amplitude value
30 which is 0 in the amplitude direction, at the half cycle point (time t_0).

[0235]

The point on this straight line and at the half cycle point (time t_0) in the coordinate space having time and amplitude value of equalized amplitude information as its coordinate axes, respectively, will hereinafter be referred to as "zero-crossing offset point".

[0236]

That is, the zero-crossing offset detecting section 301 detects an error (e.g., the arrow in Fig. 20) between the error reference point and the zero-crossing offset point as a zero-crossing offset.

[0237]

Here, it is necessary that the polarity of the amplitude value data(n-1) of the equalized amplitude information and the polarity of the amplitude value data(n) of the equalized amplitude information, in a case where a zero-crossing offset has been detected, are different.

[0238]

Note that the zero-crossing offset detecting section 301 detects a zero-crossing offset signal on the basis of equalized amplitude information and the corresponding reproduced clock. By additionally using detected data outputted from the data detecting section 35, a more accurate zero-crossing offset can be detected. This is because the detected data outputted from the data detecting section 35 have its error corrected, and this allows the zero-crossing offset detecting section 301 to detect the zero-crossing offset between the equalized amplitude information and the corresponding reproduced clock by referring to the time at which the polarities of

the error-corrected detected data switch.

[0239]

Moreover, a method of detecting a phase error in the zero-crossing offset detecting section 301 is not limited to the method described with reference to Fig. 20, but may include other schemes as well. For example, the zero-crossing offset detecting section 301 may classify equalized amplitude information, and detect a zero-crossing offset on the basis of the classified equalized amplitude information.

[0240]

Fig. 21 is a timing chart showing detection of a deviation amount and detection of a time at which the deviation is predicted to have occurred, with respect to successive synchronization patterns, in a case where a bit slip has occurred.

[0241]

"Synchronization pattern detection signal" to "synchronization counter value", and "synchronization interval" to "bit slip correction position" in Fig. 21 are similar to those in the case shown in Fig. 5, and thus their description will be omitted whenever appropriate.

[0242]

"Zero-crossing offset segment integrated value" is an integrated value of zero-crossing offset values in each of segments obtained by dividing a normal synchronization pattern interval by a predetermined number. For example, in a case where one of the segments obtained by dividing the normal synchronization pattern interval by a predetermined number equals four cycles of

the reproduced clock, the zero-crossing offset
integrating section 321 integrates zero-crossing offset
values in each segment corresponding to four cycles of
the reproduced clock, whereby to calculate a zero-
5 crossing offset segment integrated value.

[0243]

In an example shown in Fig. 21, zero-crossing
offsets are integrated in each of segments obtained by
dividing the normal synchronization pattern interval by 5.
10 After the synchronization pattern detection signal has
switched from 0 to 1, a zero-crossing offset segment
integrated value which is 0 is calculated in a first
segment which is the initial segment, and a zero-crossing
offset segment integrated value which is -2 is calculated
15 in a second segment succeeding the first segment.
Furthermore, a zero-crossing offset segment integrated
value which is 1 is calculated in a third segment
succeeding the second segment, and a zero-crossing offset
segment integrated value which is -27 is calculated in a
20 fourth segment succeeding the third segment, and further
a zero-crossing offset segment integrated value which is
20 is calculated in a fifth segment succeeding the fourth
segment.

[0244]

25 The absolute values of the zero-crossing offset
segment integrated values in the respective segments are
calculated by the bit slip judging section 311.

[0245]

In the example shown in Fig. 21, the absolute value
30 of its zero-crossing offset segment integrated value,
which is 0, is calculated in the first segment, and the

absolute value of its zero-crossing offset segment integrated value, which is 2, is calculated in the second segment. Furthermore, the absolute value of its zero-crossing offset segment integrated value, which is 1, is calculated in the third segment, the absolute value of its zero-crossing offset segment integrated value, which is 27, is calculated in the fourth segment, and the absolute value of its zero-crossing offset segment integrated value, which is 20, is calculated in the fifth segment.

[0246]

Furthermore, maximum zero-crossing offset segment integrated values in the respective segments are calculated by the bit slip judging section 311.

[0247]

In the example shown in Fig. 21, in the first segment, the initial value 0 is compared with the absolute value of its zero-crossing offset segment integrated value, which is 0, to calculate a maximum zero-crossing offset segment integrated value resulting in 0. In the second segment, the maximum zero-crossing offset segment integrated value in the first segment, which is 0, is compared with the absolute value of the zero-crossing offset segment integrated value in the second segment, which is 2, to calculate a maximum zero-crossing offset segment integrated value resulting in 2. Furthermore, in the third segment, the maximum zero-crossing offset segment integrated value in the second segment, which is 2, is compared with the absolute value of the zero-crossing offset segment integrated value in the third segment, which is 1, to calculate the maximum

zero-crossing offset segment integrated value resulting in 2, and in the fourth segment, the maximum zero-crossing offset segment integrated value in the third segment, which is 2, is compared with the absolute value of the zero-crossing offset segment integrated value in the fourth segment, which is 27, to calculate a maximum zero-crossing offset segment integrated value resulting in 27. Moreover, in the fifth segment, the maximum zero-crossing offset segment integrated value in the fourth segment, which is 27, is compared with the absolute value of the zero-crossing offset segment integrated value in the fifth segment, which is 20, to calculate the maximum zero-crossing offset segment integrated value resulting in 27.

15 [0248]

"Maximum zero-crossing offset segment integrated value time" is the heading synchronization counter value in a segment in which the absolute value of a zero-crossing offset segment integrated value is selected as a maximum zero-crossing offset segment integrated value. For example, in a case where each of segments obtained by dividing a normal synchronization pattern interval by a predetermined number equals four cycles of the reproduced clock, the maximum zero-crossing offset time storing section 322 stores the heading synchronization counter value in a segment having the maximum zero-crossing offset segment integrated value, as to the segments each corresponding to four cycles of the reproduced clock.

[0249]

30 Note that the maximum zero-crossing offset segment integrated value time is not limited to the heading

synchronization counter value in a segment in which the absolute value of a zero-crossing offset segment integrated value is selected as a maximum zero-crossing offset segment integrated value, but may also include the last synchronization counter value in the segment selected as having the maximum zero-crossing offset segment integrated value, the intermediate synchronization counter value in the segment selected as having the maximum zero-crossing offset segment integrated value, or an arbitrary synchronization counter value in the segment selected as having the maximum zero-crossing offset segment integrated value.

[0250]

In the example shown in Fig. 21, in the first segment, the heading synchronization counter value in the first segment having a maximum zero-crossing offset segment integrated value is acquired, to store a maximum zero-crossing offset segment integrated value time which is 0 in the maximum zero-crossing offset time storing section 322. In the second segment, the absolute value of its zero-crossing offset segment integrated value is selected as a maximum zero-crossing offset segment integrated value, and thus the heading synchronization counter value in the second segment is acquired, to store a maximum zero-crossing offset segment integrated value time which is 4 in the maximum zero-crossing offset time storing section 322.

[0251]

Furthermore, in the third segment, the absolute value of its zero-crossing offset segment integrated value is not selected as a maximum zero-crossing offset

segment integrated value, and thus the maximum zero-crossing offset segment integrated value time stored in the maximum zero-crossing offset time storing section 322 remains unchanged. In the fourth segment, the absolute value of its zero-crossing offset segment integrated value is selected as a maximum zero-crossing offset segment integrated value, and thus the heading synchronization counter value in the fourth segment is acquired, to store a maximum zero-crossing offset segment integrated value time which is 12 in the maximum zero-crossing offset time storing section 322. And in the fifth segment, the absolute value of its zero-crossing offset segment integrated value is not selected as a maximum zero-crossing offset segment integrated value, and thus the maximum zero-crossing offset segment integrated value time stored in the maximum zero-crossing offset time storing section 322 remains unchanged.

[0252]

In the example shown in Fig. 21, bit slip correction amounts are calculated as follows. A bit slip correction amount which is 0 is calculated in a synchronization pattern interval $(k-1, k)$, i.e., at a time $k-1$, and a normal synchronization interval which is 20 is subtracted from a synchronization interval which is 19 in a synchronization pattern interval $(k, k+1)$, whereby to calculate a bit slip correction amount resulting in -1 at a time k .

[0253]

"Bit slip correction position" is a maximum zero-crossing offset segment integrated value time stored in the maximum zero-crossing offset time storing section 322

upon rise of a synchronization pattern detection signal.
[0254]

That is, the bit slip correction position represents a time for a segment in which a deviation of
5 detected data (equalized amplitude information) is assumed to have occurred with respect to the corresponding reproduced clock.
[0255]

In the example shown in Fig. 21, bit slip
10 correction positions are calculated as follows. A bit slip correction position which is 1 is calculated at the time $k-1$, and a bit slip correction position resulting in 12 is calculated at the time k .
[0256]

15 In the example shown in Fig. 21, the bit slip correction amount which is -1 and the bit slip correction position which is 12 are supplied to a FIFO control section 82 as the bit slip correction information, in the synchronization pattern interval $(k, k+1)$. Moreover, the
20 bit slip judging section 311 judges that a bit slip has occurred since the bit slip correction amount, i.e., the deviation amount is other than 0.
[0257]

Note that in the synchronization pattern interval
25 $(k-1, k)$, the bit slip correction amount equals 0, and the bit slip correction position equals 1. In this case, however, no bit slip correction is made, since the bit slip correction amount is 0, although the bit slip correction position takes a certain value.
30 [0258]

Fig. 22 is a diagram showing a method of

calculating a bit slip occurrence position (a time for a segment in which a deviation of detected data (equalized amplitude information) is assumed to have occurred with respect to the corresponding reproduced clock) in a case
5 where a bit slip has occurred.

[0259]

In Fig. 22, a mutual relationship is shown among "zero-crossing offset segment integrated value", "detected data", "absolute value of zero-crossing offset
10 segment integrated value", "detected data after correction" and "detected data range for correction" in segments N-1, N and N+1 each defined by synchronization pattern detection signals. Moreover, in an example shown in Fig. 22, a bit slip has occurred at a time A.

15 [0260]

"Detected data", and "detected data after correction" and "detected data range for correction" in Fig. 22 are similar to those in the case shown in Fig. 6, and thus their description will be omitted whenever
20 appropriate.

[0261]

A waveform 411 represents integrated values of zero-crossing offsets, calculated by the zero-crossing offset integrating section 321. Rectangles shown in a
25 manner overlapping with the waveform 411 respectively represent integrated values of zero-crossing offsets in respective segments.

[0262]

Since the absolute value of a zero-crossing offset
30 segment integrated value is an absolute value as to a zero-crossing offset segment integrated value, a zero-

crossing offset segment integrated value which is a negative value becomes a positive value with its sign inverted. Furthermore, through a comparison among the absolute values of zero-crossing offset segment
5 integrated values, the absolute value of a zero-crossing offset segment integrated value in a segment denoted by B becomes the maximum zero-crossing offset segment integrated value, and thus (a time for) the segment denoted by B becomes the bit slip correction position.
10 [0263]

The detected data is corrected into as many detected data bits as those to be arranged between two normal synchronization patterns in a case where no bit slip occurs. In the example shown in Fig. 22, the
15 "detected data after correction" is corrected so as to have L channel bits.
[0264]

As a result of this correction, the detected data from the time for the segment denoted by B to the end of
20 the segment N are corrected. In a segment 412 with large zero-crossing offsets, the reproduced signals themselves have changed, and thus, even if a correction is made in the time direction, normal detected data cannot be obtained. In a segment 413 with small zero-crossing
25 offsets, the reproduced signals themselves have recovered, and thus normal detected data can be obtained by a correction in the time direction.
[0265]

Thus, in a case where a burst error has occurred
30 and a bit slip has occurred due to the burst error, the reproducing apparatus of the present invention can

correct an error preceding a synchronization pattern which is detected after the bit slip.

[0266]

Fig. 23 is a timing chart for explaining insertion
5 of a synchronization pattern detection signal in a case where no synchronization pattern has been detected in the synchronization pattern interpolation mode.

[0267]

"Synchronization pattern detection signal" to
10 "reproduced clock", and "synchronization counter value" to "bit slip correction position" in Fig. 23 are similar to those shown in Fig. 21, and thus their description will be omitted whenever appropriate.

[0268]

15 In an example shown in Fig. 23, zero-crossing offset segment integrated values are obtained as follows. In segments obtained by dividing a "synchronization pattern interval after interpolation" $(k-1, k)$ by 5, zero-crossing offsets are integrated, and in segments
20 obtained by dividing a "synchronization pattern interval after interpolation" $(k, k+1)$ by 6, zero-crossing offsets are integrated.

[0269]

In a "synchronization pattern interval after
25 interpolation" $(k-1, k)$, after a "synchronization pattern detection signal after interpolation" has switched from 0 to 1, in a first segment which is the initial segment, a zero-crossing offset segment integrated value which is 0 is calculated, and in a second segment succeeding the
30 first segment, a zero-crossing offset segment integrated value which is -1 is calculated. Furthermore, a zero-

crossing offset segment integrated value which is 1 is calculated in a third segment succeeding the second segment, a zero-crossing offset segment integrated value which is -4 is calculated in a fourth segment succeeding the third segment, and a zero-crossing offset segment integrated value which is 2 is calculated in a fifth segment succeeding the fourth segment.

[0270]

Furthermore, after the "synchronization pattern detection signal after interpolation" has switched from 0 to 1 in a "synchronization pattern interval after interpolation" $(k, k+1)$, a zero-crossing offset segment integrated value which is -2 is calculated in a first segment which is the initial segment, and a zero-crossing offset segment integrated value which is 1 is calculated in a second segment succeeding the first segment. Furthermore, a zero-crossing offset segment integrated value which is 1 is calculated in a third segment succeeding the second segment, a zero-crossing offset segment integrated value which is -1 is calculated in a fourth segment succeeding the third segment, and a zero-crossing offset segment integrated value which is 1 is calculated in a fifth segment succeeding the fourth segment. Moreover, due to a bit slip having occurred, in a sixth segment succeeding the fifth segment, a zero-crossing offset integrated value which is 0 is calculated.

[0271]

As the absolute values of the zero-crossing offset segment integrated values, in the synchronization pattern interval $(k-1, k)$ in the example shown in Fig. 23, the absolute value of its zero-crossing offset segment

integrated value, which is 0, is calculated in the first segment, and the absolute value of its zero-crossing offset segment integrated value, which is 1, is calculated in the second segment. Furthermore, the absolute value of its zero-crossing offset segment integrated value, which is 1, is calculated in the third segment, the absolute value of its zero-crossing offset segment integrated value, which is 4, is calculated in the fourth segment, and the absolute value of its zero-crossing offset segment integrated value, which is 2, is calculated in the fifth segment.

[0272]

Furthermore, in the synchronization pattern interval $(k, k+1)$, the absolute value of its zero-crossing offset segment integrated value, which is 2, is calculated in the first segment, the absolute value of its zero-crossing offset segment integrated value, which is 1, is calculated in the second segment, the absolute value of its zero-crossing offset segment integrated value, which is 1, is calculated in the third segment, the absolute value of its zero-crossing offset segment integrated value, which is 1, is calculated in the fourth segment, the absolute value of its zero-crossing offset segment integrated value, which is 1, is calculated in the fifth segment, and the absolute value of its zero-crossing offset segment integrated value, which is 0, is calculated in the sixth segment.

[0273]

As maximum zero-crossing offset segment integrated values, in the synchronization pattern interval $(k-1, k)$ in the example shown in Fig. 23, the initial value 0 is

compared with the absolute value of its zero-crossing
 offset segment integrated value, which is 0, to calculate
 a maximum zero-crossing offset segment integrated value
 resulting in 0, in the first segment. In the second
 5 segment, the maximum zero-crossing offset segment
 integrated value in the first segment, which is 0, is
 compared with the absolute value of the zero-crossing
 offset segment integrated value in the second segment,
 which is 1, to calculate a maximum zero-crossing offset
 10 segment integrated value resulting in 1. Furthermore, in
 the third segment, the maximum zero-crossing offset
 segment integrated value in the second segment, which is
 1, is compared with the absolute value of the zero-
 crossing offset segment integrated value in the third
 15 segment, which is 1, to calculate the maximum zero-
 crossing offset segment integrated value resulting in 1,
 and in the fourth segment, the maximum zero-crossing
 offset segment integrated value in the third segment,
 which is 1, is compared with the absolute value of the
 20 zero-crossing offset segment integrated value in the
 fourth segment, which is 4, to calculate a maximum zero-
 crossing offset segment integrated value resulting in 4.
 Moreover, in the fifth segment, the maximum zero-crossing
 offset segment integrated value in the fourth segment,
 25 which is 4, is compared with the absolute value of the
 zero-crossing offset segment integrated value in the
 fifth segment, which is 2, to calculate the maximum zero-
 crossing offset segment integrated value resulting in 4.
 [0274]

30 Furthermore, in the synchronization pattern
 interval $(k, k+1)$, in the first segment, the initial

value 0 is compared with the absolute value of its zero-crossing offset segment integrated value, which is 2, to calculate a maximum zero-crossing offset segment integrated value resulting in 2. In the second segment, the maximum zero-crossing offset segment integrated value in the first segment, which is 2, is compared with the absolute value of the zero-crossing offset segment integrated value in the second segment, which is 1, to calculate the maximum zero-crossing offset segment integrated value resulting in 2. Furthermore, in the third segment, the maximum zero-crossing offset segment integrated value in the second segment, which is 2, is compared with the absolute value of the zero-crossing offset segment integrated value in the third segment, which is 1, to calculate the maximum zero-crossing offset segment integrated value resulting in 2, and in the fourth segment, the maximum zero-crossing offset segment integrated value in the third segment, which is 2, is compared with the absolute value of the zero-crossing offset segment integrated value in the fourth segment, which is 1, to calculate the maximum zero-crossing offset segment integrated value resulting in 2.

[0275]

Moreover, in the fifth segment, the maximum zero-crossing offset segment integrated value in the fourth segment, which is 2, is compared with the absolute value of the zero-crossing offset segment integrated value in the fifth segment, which is 1, to calculate the maximum zero-crossing offset segment integrated value resulting in 2, and in the sixth segment, the maximum zero-crossing offset segment integrated value in the fifth segment,

which is 2, is compared with the absolute value of the zero-crossing offset segment integrated value in the sixth segment, which is 0, to calculate the maximum zero-crossing offset segment integrated value resulting in 2.

5 [0276]

In the synchronization pattern interval (k-1, k) in the example shown in Fig. 23, as maximum zero-crossing offset segment integrated value times, in the example shown in Fig. 23, in the first segment, the heading
 10 synchronization counter value in the first segment having a maximum zero-crossing offset segment integrated value is acquired, to store a maximum zero-crossing offset segment integrated value time which is 0 in the maximum zero-crossing offset time storing section 322. In the
 15 second segment, the absolute value of a zero-crossing offset segment integrated value error is selected as a maximum zero-crossing offset segment integrated value, and thus the heading synchronization counter value in the second segment is acquired, to store a maximum zero-
 20 crossing offset segment integrated value time which is 4 in the maximum zero-crossing offset time storing section.
 [0277]

Furthermore, in the third segment, the absolute value of a zero-crossing offset segment integrated value
 25 error is selected as a maximum zero-crossing offset segment integrated value, and thus the heading synchronization counter value in the third segment having the maximum zero-crossing offset segment integrated value is acquired, to store a maximum zero-crossing offset
 30 segment integrated value time which is 8 in the maximum zero-crossing offset time storing section. In the fourth

segment, the absolute value of a zero-crossing offset segment integrated value error is selected as a maximum zero-crossing offset segment integrated value, and thus the heading synchronization counter value in the fourth segment having the maximum zero-crossing offset segment integrated value is acquired, to store a maximum zero-crossing offset segment integrated value time which is 12 in the maximum zero-crossing offset time storing section. And in the fifth segment, the absolute value of a zero-crossing offset segment integrated value error is not selected as a maximum zero-crossing offset segment integrated value, and thus the maximum zero-crossing offset segment integrated value time stored in the maximum zero-crossing offset time storing section 322 remains unchanged.

[0278]

Furthermore, in the synchronization pattern interval $(k, k+1)$ in the example shown in Fig. 23, as maximum zero-crossing offset segment integrated value times, in the first segment, the heading synchronization counter value in the first segment having a maximum zero-crossing offset segment integrated value is acquired, to store a maximum zero-crossing offset segment integrated value time which is 0 in the maximum zero-crossing offset time storing section 322. In the second segment, the absolute value of a zero-crossing offset segment integrated value error is not selected as a maximum zero-crossing offset segment integrated value, and thus the maximum zero-crossing offset segment integrated value time stored in the maximum zero-crossing offset time storing section 322 remains unchanged. In the third

segment, the absolute value of a zero-crossing offset segment integrated value error is not selected as a maximum zero-crossing offset segment integrated value, and thus the maximum zero-crossing offset segment
5 integrated value time stored in the maximum zero-crossing offset time storing section 322 remains unchanged.

[0279]

In the fourth segment, the absolute value of a zero-crossing offset segment integrated value error is
10 not selected as a maximum zero-crossing offset segment integrated value, and thus the maximum zero-crossing offset segment integrated value time stored in the maximum zero-crossing offset time storing section 322 remains unchanged. In the fifth segment, the absolute
15 value of a zero-crossing offset segment integrated value error is not selected as a maximum zero-crossing offset segment integrated value, and thus the maximum zero-crossing offset segment integrated value time stored in the maximum zero-crossing offset time storing section 322
20 remains unchanged. And in the sixth segment, the absolute value of a zero-crossing offset segment integrated value error is not selected as a maximum zero-crossing offset segment integrated value, and thus the maximum zero-crossing offset segment integrated value
25 time stored in the maximum zero-crossing offset time storing section 322 remains unchanged.

[0280]

Note that in a case where maximum zero-crossing offset segment integrated values are equal in successive
30 segments, which one of the former and latter maximum zero-crossing offset segment integrated values should

prevail is determined by setting. In the example shown in Fig. 23, the maximum zero-crossing offset segment integrated values in the second and third segments are 1, and the maximum zero-crossing offset segment integrated value time in the third segment is 8. Here, if the maximum zero-crossing offset segment integrated values are equal, it is set such that the latter maximum zero-crossing offset segment integrated value should prevail, and thus the value in the third segment prevails over that in the second segment.

[0281]

In the example shown in Fig. 23, bit slip correction amounts are calculated as follows. In the "synchronization pattern interval after correction" ($k-1$, k), i.e., at the time $k-1$, a bit slip correction amount which is 0 is calculated, and in the "synchronization pattern interval after correction" (k , $k+1$), i.e., at the time k , a bit slip correction amount which is 0 is calculated. Moreover, in a "synchronization pattern interval after correction" ($k+1$, $k+2$), i.e., at a time $k+1$, a bit slip correction amount which is 1 is calculated.

[0282]

Here, for example, at the time k , the synchronization pattern detection signal inserting section 85 inserts the synchronization pattern detection signal at the predetermined time, and thus 0 is calculated as the bit slip correction amount at the time k .

[0283]

In the example shown in Fig. 23, bit slip

correction positions are calculated as follows. At the time $k-1$, a bit slip correction position which is 0 is calculated, and at the time k , a bit slip correction position which is 12 is calculated. And further, at the time $k+1$, a bit slip correction position which is 0 is calculated.

[0284]

In a case where the synchronization pattern detection signal inserting section 85 has inserted a synchronization pattern detection signal at a predetermined time, a bit slip correction is made at a time at which a first synchronization pattern detection signal is detected after the synchronization pattern detection signal has been inserted. In the example shown in Fig. 23, at the time $k+1$, which is after the time k at which the synchronization pattern detection signal has been inserted, a bit slip correction is made. And the bit slip correction amount which is 1 and the bit slip correction position which is 12 are supplied to the FIFO control section 82 as the bit slip correction information. In this case, the bit slip judging section 311 judges that a bit slip has occurred because the bit slip correction amount, i.e., the deviation amount is other than 0.

[0285]

Note that at the time k , the bit slip correction amount equals 0, and the bit slip correction position equals 12. In this case, however, no bit slip correction is made, since the bit slip correction amount is 0, although the bit slip correction position takes a certain value.

[0286]

Fig. 24 is a diagram showing a method of calculating a bit slip occurrence position in a case where a bit slip has occurred and no synchronization pattern has been detected.

[0287]

In Fig. 24, a mutual relationship is shown among "zero-crossing offset segment integrated value", "detected data", "absolute value of zero-crossing offset segment integrated value", "detected data after correction" and "detected data range for correction" in segments N-1, N and N+1 each defined by synchronization pattern detection signals.

[0288]

"Zero-crossing offset segment integrated value" to "detected data range for correction" in Fig. 24 are similar to those in the case shown in Fig. 22, and thus their description will be omitted whenever appropriate.

[0289]

Similarly to the case shown in Fig. 22, rectangles shown in a manner overlapping with a waveform 411 respectively represents zero-crossing offset segment integrated values. That is, in an example shown in Fig. 24, a synchronization pattern detection signal is inserted at a time at which the segment N switches to the segment N+1, and the rectangles shown so as to overlap with the waveform 411 respectively represent zero-crossing offset integrated values in segments, in the segment N+1 after the synchronization pattern detection signal has been inserted.

[0290]

As to "detected data", in the example shown in Fig. 24, L channel bit detected data is arranged in the segment N-1 in which no bit slip has occurred. Moreover, in the segments N and N+1, a bit slip has occurred, and thus no synchronization pattern has been detected. Consequently, through the segments N and N+1, detected data of (L+L+1) channel bit is arranged.

[0291]

In the example shown in Fig. 24, in the segment N+1 after the synchronization pattern detection signal has been inserted, the absolute value of a zero-crossing offset segment integrated value in a segment denoted by C becomes maximum, and thus (a time for) the segment denoted by C is the bit slip correction position.

[0292]

As to "detected data after interpolation", in the example shown in Fig. 24, in the segment N in which no bit slip is deemed to have occurred, bit detected data of L channel is arranged. In other words, since the synchronization pattern detection signal is inserted, detected data of L channel bit is arranged in the segment N, and the detected data of remaining (L+1) channel bit is arranged in the segment N+1.

[0293]

Then, in the segment N+1, the detected data of (L+1) channel bit is changed to data of L channel bit by correction.

[0294]

That is, bit slip correction is executed such that the detected data in the segment N+1 equals L channel bits.

[0295]

As to "detection data range for correction", the reproduced signals themselves have changed in the segment 421, and thus, even if they are corrected in the time direction, normal detected data cannot be obtained. Since the reproduced signal themselves have recovered in the segment 422, normal detected data can be detected by making a correction in the time direction.

[0296]

Thus, in a case where no synchronization pattern has been detected, the invention apparatus of the present invention inserts a synchronization pattern detection signal at a predetermined time, to supplement a synchronization pattern, whereby it can correct an error preceding the synchronization pattern which is detected after a bit slip.

[0297]

Referring to flowcharts in Figs. 25 to 27, processing will be described, which is performed by the reproducing apparatus that executes a correction program by using zero-crossing offsets.

[0298]

Fig. 25 is a flowchart for explaining a reproduction process by the reproducing apparatus.

[0299]

Steps S101 to S105 are similar to steps S1 to S5 in Fig. 9, respectively, and thus their description will be omitted.

[0300]

In step S106, a bit slip correcting process using zero-crossing offsets is executed, after which the

process returns to step S101, to repeat the above-mentioned processing.

[0301]

5 Details of the bit slip correcting process using zero-crossing offsets in step S106 will be described with reference to the flowchart shown in Fig. 26.

[0302]

10 Steps S121, S123 and S125 are similar to steps S21, S23 and S25 in Fig. 10, respectively, and thus their description will be omitted.

[0303]

15 In step S122, the zero-crossing offset detecting section 301 detects a zero-crossing offset on the basis of equalized amplitude information supplied from the equalizer 34 and the corresponding reproduced clock supplied from the clock generating section 33, and supplies a zero-crossing offset signal representing the zero-crossing offset to the bit slip correcting section 302.

20 [0304]

In step S124, the bit slip correcting section 302 executes a correction information calculating process.

[0305]

25 Details of the correction information calculating process in step S124 will be described with reference to the flowchart of Fig. 27.

[0306]

30 In step S141, the zero-crossing offset integrating section 321 integrates zero-crossing offsets detected in each of predetermined segments, to calculate a zero-crossing offset segment integrated value.

[0307]

In step S142, the bit slip judging section 311 detects a maximum for the absolute values of the zero-crossing offset segment integrated values.

5 [0308]

In step S143, the maximum zero-crossing offset time storing section 322 detects a bit slip correction position which is a time at which the maximum absolute value of the zero-crossing offset segment integrated
10 value has been detected, after which the process is terminated.

[0309]

Returning to Fig. 26 again, step S125 is executed, after which the bit slip correcting process is terminated.

15 [0310]

As mentioned above, the reproducing apparatus executes the correction program by using zero-crossing offsets.

[0311]

20 Note that in the above-mentioned examples, a description of detecting an error between the error reference point and the phase error point (or the zero-crossing offset point) has been given as the error detecting process. However, in the present invention, it
25 may alternatively be configured to detect an error between the error reference point and any of points on a straight line connecting a point specified by the start time of a certain cycle of the reproduced clock and an amplitude value data(n-1) of equalized amplitude
30 information at that start time, with a point specified by the start time of a next cycle of the reproduced clock

and an amplitude value data(n) of equalized amplitude information at the start time of the next cycle, in a coordinate space having time and amplitude value of equalized amplitude information as its coordinate values, respectively.

[0312]

That is, it may be configured to detect an error between the error reference point and a value based on the amplitude values of two adjacent equalized amplitude information bits.

[0313]

Moreover, the process of detecting a zero-crossing offset is not limited to the examples described above. For example, a zero-crossing offset may be detected by a sampling process in which a sampling frequency is doubled for oversampling, whereby to detect an amplitude value of equalized amplitude information at the half cycle point.

[0314]

Furthermore, the method of detecting an amplitude value of equalized amplitude information at the half cycle point is not limited to oversampling, but may include interpolation as well. Furthermore, it may also be configured to detect an amplitude value of equalized amplitude information at the half cycle point by adding an A/D converter dedicated to such detection.

[0315]

The series of processes described above can be performed by hardware, but by software as well. In a case of performing the processes depending on software, a program constituting the software is installed into a computer incorporated into dedicated hardware, or, e.g.,

a general-purpose computer that can perform various processing by installing various programs, from a recording medium.

[0316]

5 This recording medium may include, as shown in Fig. 2 or 18, separately from the computer, not only package media, such as the magnetic disk 71 (including a flexible disk), the optical disc 72 (including a CD-ROM (Compact Disc-Read Only Memory), a DVD (Digital Versatile Disc)),
10 the magneto-optical disc 73 (including a MD (Mini-Disc) (trademark)), or the semiconductor memory 74, which is distributed to provide a user with the program and which has the program recorded therein, but also a ROM having the program recorded therein, a hard disk included in a
15 storing section, or the like which is provided with the user as incorporated into the computer.

[0317]

 Note that it may also be configured such that the program for executing the above-mentioned series of
20 processes is installed into the computer through a wired or wireless communication medium, such as a local area network, the Internet or digital satellite broadcasting, via a router, a modem or the like, as necessary.

[0318]

25 Moreover, the steps describing the program stored in the recording medium may include processes performed not only time-sequentially according to a sequence described, but also processes executed parallelly or individually, if not necessarily time-sequentially.